

MIPI CSI Video Output Board
[SVO-06 CSI]
Hardware Specification

Rev.1.0

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	27. Jun., 2024	New File (Equivalent to Japanese version 1.2)	R. Sugo

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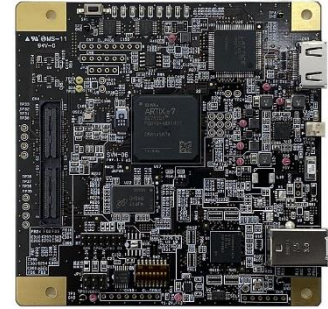
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1. Overview

This document is a hardware specification of the "SVO-06 CSI" to convert video signals input via USB 3.0 to the MIPI CSI standard video signal. This board can send free video signals to devices and ICs that have MIPI CSI input. It is possible to adjust the format and output timing of the video signal using a PC.



This board operates according to the operation mode specified by DIP SW (SW2). In the standard specification, there are two modes, "USB mode" and "Updater mode".

1.1. SVO-06 CSI Functions

USB mode: Video files on a computer -> MIPI CSI video signal conversion

Updater mode: Update the board firmware

1.2. Specifications (USB Mode)

- Power: USB bus supply (external power input applicable) / +5V 0.7A typ.
- Output Standard: MIPI CSI video signal (4 data lanes + 1 clock lane)
 - Data rate per lane: 400 ~ 1500 Mbps
 - Effective pixel data rate: Max. 6.0 Gbps
 - MIPI clock frequency: 200 ~ 750 MHz
 - MIPI data lane: 2 lane / 4 lane supported
- Output Resolution: Max. (width x height) pixel
 - Width = 8190
 - Height = 4095
- Output Pixel Format: YUV4:2:2 8-bit, Raw8, Raw10, Raw12, Raw20, RGB24
- Input: USB 3.0
- Input Through Rate (USB): Max. 3.0 Gbps
- Input Resolution: Same as output resolution
- Output Frame Rate: Can be set freely
- Input Pixel Format (USB): Same as output pixel format

If the input format is AVI, the pixel format on the file header supports YUV or RGB24 (DIB).
By storing the contents of the frame data in RAW, it is possible to output video in RAW format.

1.3. Board Specification Table

Items		Contents	Remarks
Video Input Interface		USB 3.0 (Windows)	
Video Output Interface		MIPI CSI video signal	Non-Continuous / Continuous Clock supported. 4 data lanes + 1 clock lane
Input Resolution		Max. 8190 x 4095 pixel Within 6.0 Gbps	
Output Resolution		Max. 8190 x 4095 pixel	
Sync Signal		FS / FE	
MIPI Data Lane		2, 4 lanes	1, 3 lanes are unsupported.
Data Rate per Lane		400 ~ 1500 Mbps	
Supported Pixel Formats		YUV4:2:2 8bit / RGB24 / Raw8 / Raw10 / Raw12 / Raw16 / Raw20	
Other IF	I2C	1 system	SCL frequency 100 / 200 / 400 kHz
	GPIO	16bit	IN / OUT can be switched for each bit.
Input Power		+5V ($\pm 5\%$)	Use either USB bus power or 2pin connector.
Output Power		VDDIO output (1.8V, 2.5V, 3.3V) 5V, 3.3V, 1.2V output	Since it is shared with the internal power supply, we recommend to use a current of 150mA or less each. Current ratings are 800mA (1.8, 2.5, 3.3V) and 500mA (1.2V, 5V).
Other Functions		Video output timing can be set in pixel clock units, including blank periods.	Virtual Channel 0~3 are supported.
Interface Connector		120 Pin (QSH-060-01-L-D-A-K-TR)	
FPGA		Artix-7 (XC7A35T) CrossLink (LIF-MD6000)	
Frame Memory		256MB (DDR3 SDRAM)	
USB3.0 Chip		Infineon EZ-USB FX3	

Items	Contents	Remarks
Board Dimensions	101.6 x 101.6 x 25.7 [mm]	Length x Width x Height
Attached Software (Windows)	NVFilePlayer SVMUpdater	
Supported Serializer Board Examples	GMO-9295A-F / GMO-96717	

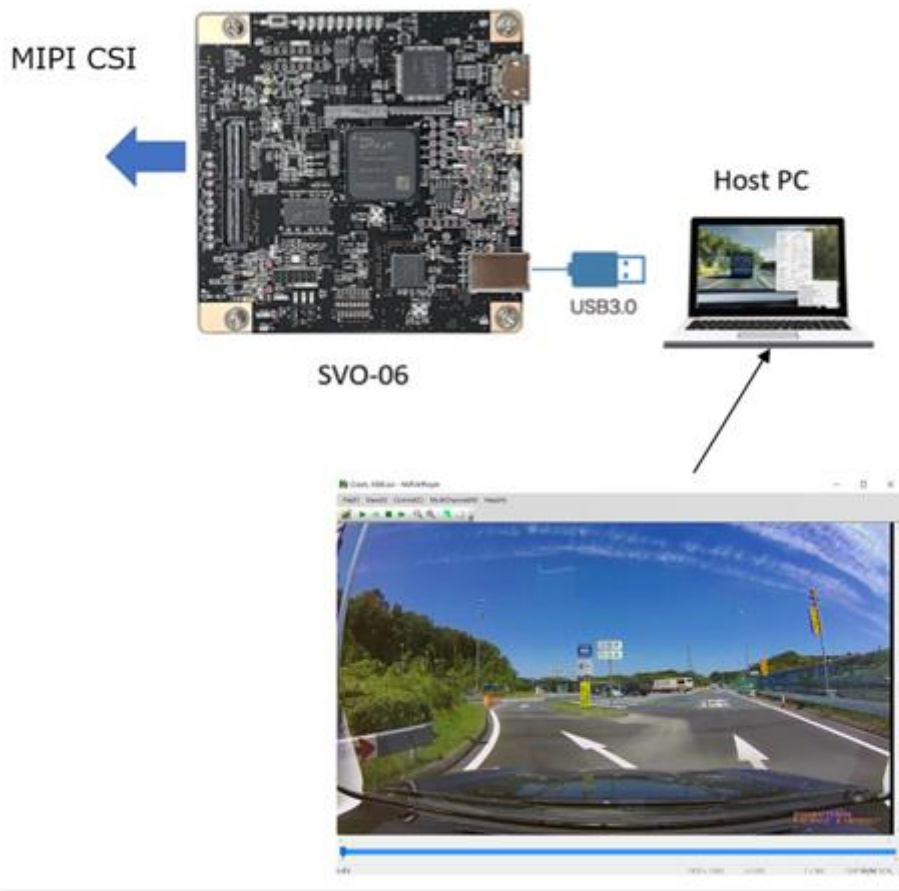
2. USB Mode Operation Details

This chapter describes USB mode (USB input, MIPI CSI output). When the power is turned on with the DIP SW set to 7: OFF and 8: ON, it starts in USB mode.

2.1. Functions and Features in USB Mode

- Converts uncompressed .avi or .frm files stored on a PC into MIPI CSI video signals.
- Supports Windows OS.
- Controlled by dedicated video output software (NVFilePlayer). Please refer to the “NVFilePlayer Software Manual”.
- The following settings can be made using the software.
 - Effective area size, blank timing and frame rate of an output video.
 - The number of MIPI lanes, bit rate per lane and continuous / non-continuous of clock lane.
 - The data type for output video can select from YUV 4:2:2 8-bit, Raw 8 ~ 20, and RGB 24.
 - Virtual Channel of output video can select from 0, 1, 2, 3.
- The USB3.0 chip is Infineon EZ-USB FX3.
- When power is turned on with the DIP SW set to 7: OFF and 8: ON, this board starts in USB mode.

2.2. Connection Example in USB Mode

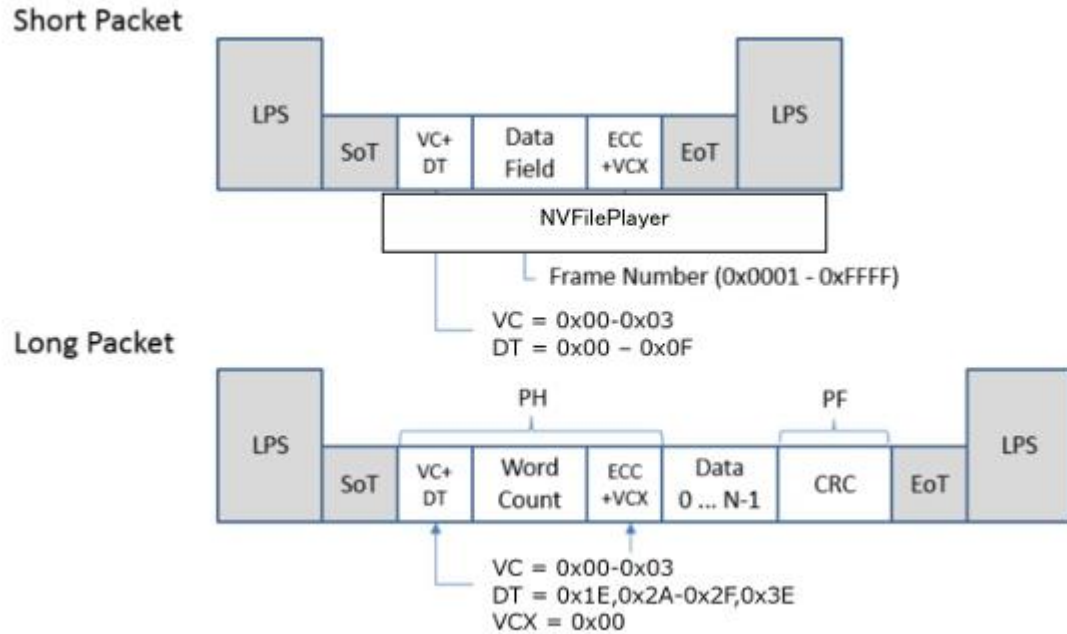


The above figure is an example of a connection configuration.

In USB mode, the PC software "NVFilePlayer" loads video data such as .avi files and sends them to the SVO-06.

2.3. Output Format

Details of the MIPI CSI signals output are shown below.

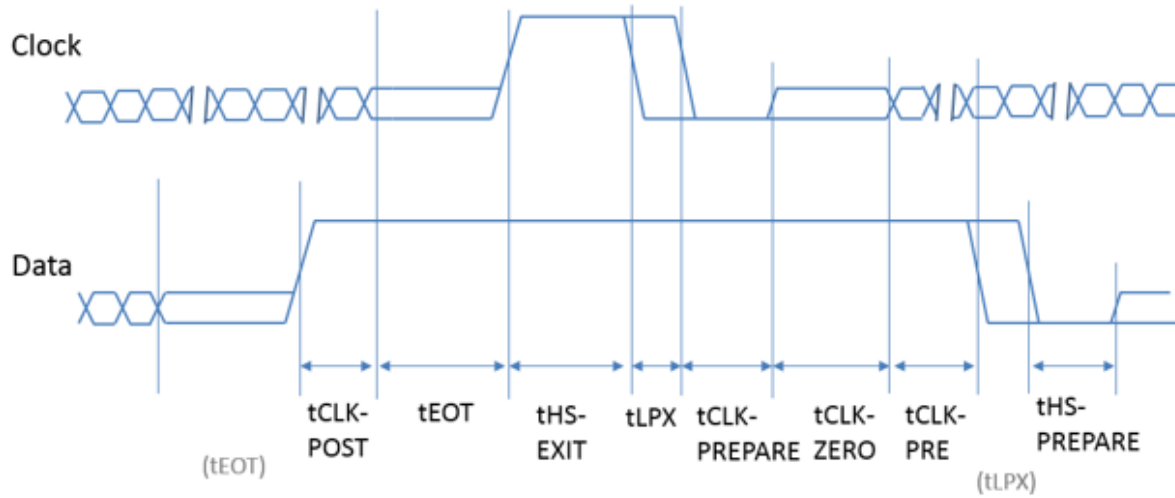


The table below lists the pixel formats and Long Packet Data Types supported by this board. The Input AVI Format column indicates the pixel format of the input AVI file when running this board with NVFilePlayer.

Pixel Format	Data Type (DT)	Input AVI Format (NVFilePlayer)
16-bit YCbCr 4:2:2 Format	0x1E	UYVY, YUY2
24-bit RGB 8-8-8 Format	0x3E	DIB (Upside down)
Raw8	0x2A	UYVY
Raw10	0x2B	UYVY
Raw12	0x2C	UYVY
Raw16	0x2E	UYVY
Raw20	0x2F	DIB (Upside down)

- Even if you import AVI data of DIB or RGB, the order of the data to be sent is always from the beginning of the AVI file first.

2.4. MIPI Output Timing

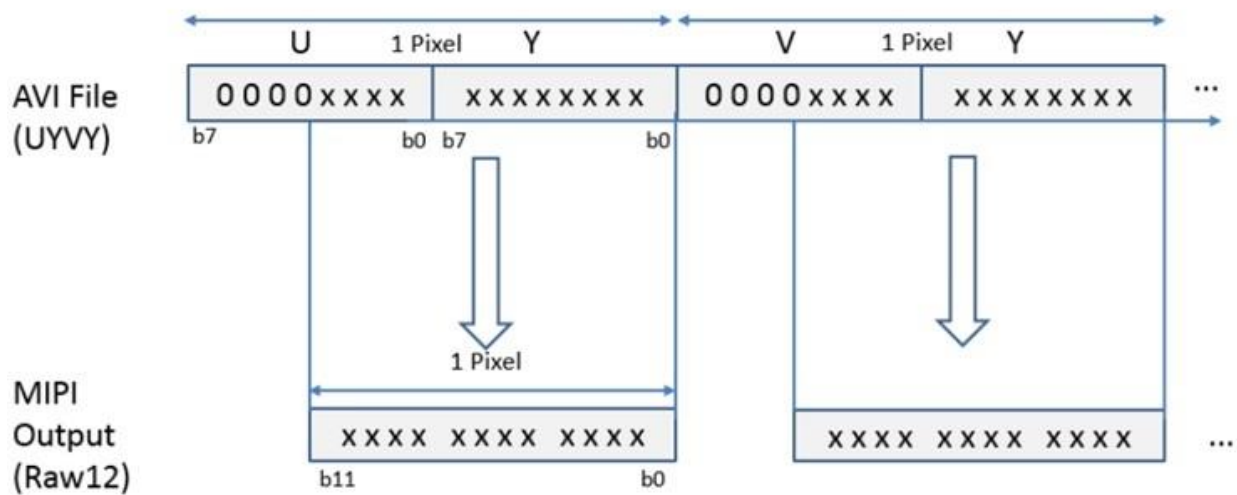


Timing	Measured Value - 1	Measured Value - 2	Measured Value - 3
$t_{\text{CLK-POST}}$	720ns	360ns	220ns
t_{EOT}	210ns	105ns	75ns
$t_{\text{HS-EXIT}}$	-	-	-
t_{LPX}	95ns	95ns	95ns
$t_{\text{CLK-PREPARE}}$	75ns	75ns	50ns
$t_{\text{CLK-PREPARE}} + t_{\text{CLK-ZERO}}$	1050ns	525ns	310ns
$t_{\text{CLK-PRE}}$	300ns	150ns	110ns
$t_{\text{HS-PREPARE}}$	55ns	55ns	55ns

- Measured value – 1: Indicates the measured value at 500Mbps/lane output.
- Measured value – 2: Indicates the measured value at 1000Mbps/lane output.
- Measured value – 3: Indicates the measured value at 1500Mbps/lane output.
- It is possible to fine-tune each timing as a customization, please contact us if you would like to do this.

2.5. Processing on RAW Output

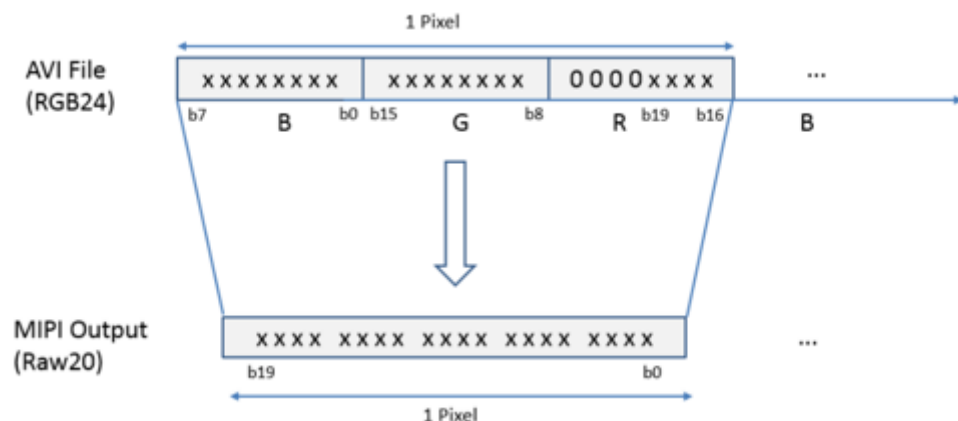
SVO-06 supports output of Raw formats (Raw8 / Raw10 / Raw12 / Raw16 / Raw20). However, the VFW of standard Windows OS does not support Raw formats. When you select the Raw output in USB mode, input files follow the format saved by our capture boards such as SVM-06. In this case, the MIPI signals are output assuming that valid data is stored as part of the input data in YUV or RGB format. The details of the data format are as follows.



The host side treats it as UYVY and padded with 0 for the upper bits.

(Bit rate is 4/3 times.)

*The above figure shows Raw12, and other Raws are similar.



The host side treats it as RGB24 and padded with 0 for the upper bits.

(Bit rate is 6/5 times.)

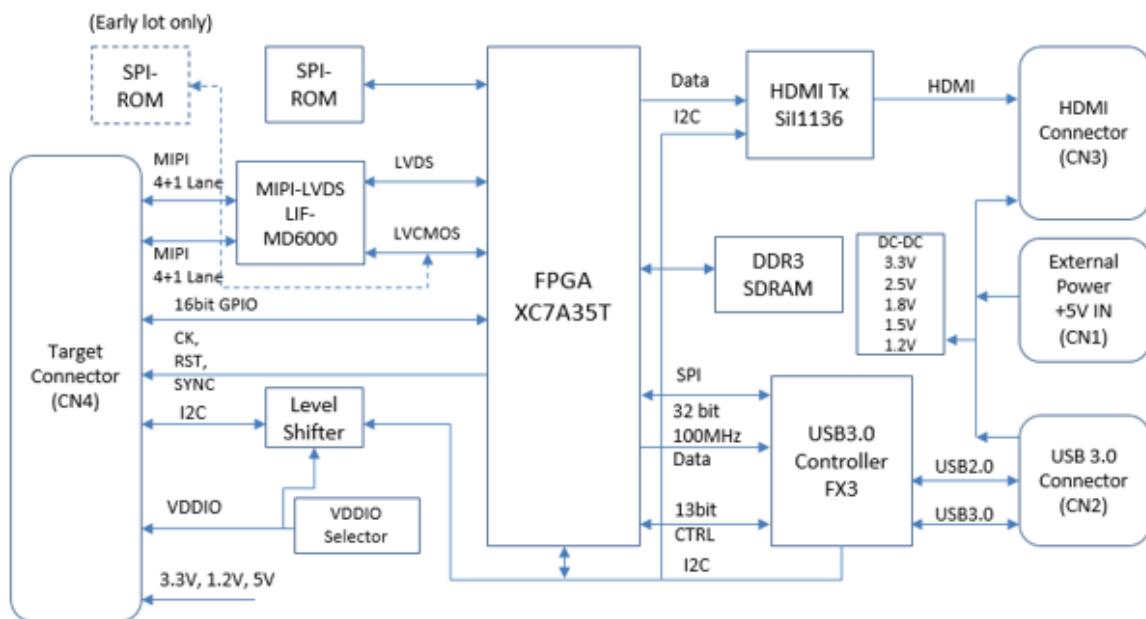
For RGB24 and Raw20 output, the RGB24 format is supported as input AVI files. SVO-06 always outputs pixels in the same order as the byte array in the AVI file. When emulating a standard camera using an AVI file with RGB24, the vertical direction of each frame in the AVI file is different from the order from bottom-left to top-right of VFW with RGB24. The data must be stored in the order from top-left to bottom-right.

In other words, if you use an AVI file in RGB24 which is upside-down, the board outputs signals in the order of top-left pixels to bottom-right pixels.

3. Block Diagram of SVO-06

A schematic block diagram of the SVO-06 is shown below.

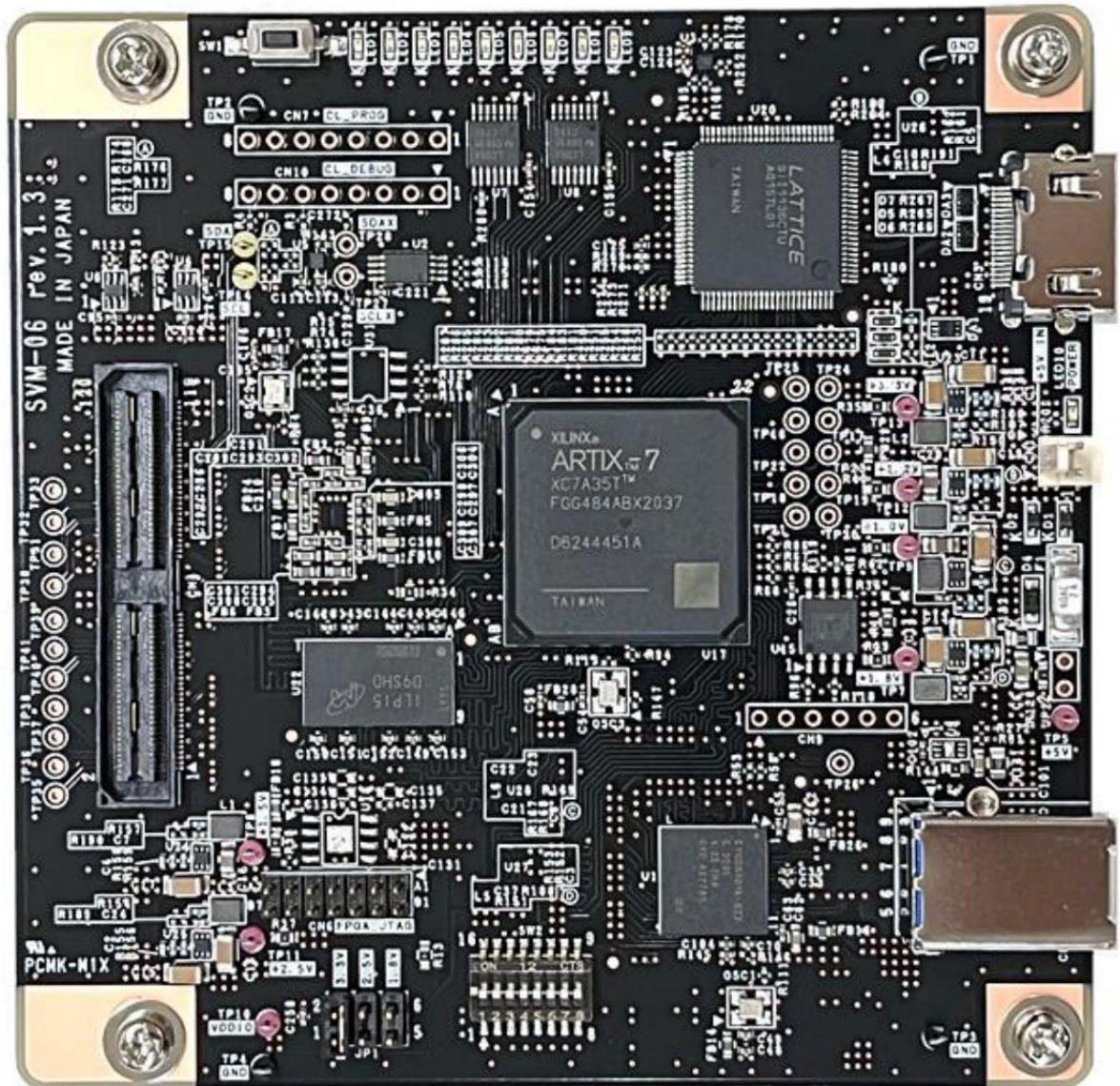
3.1. Block Diagram



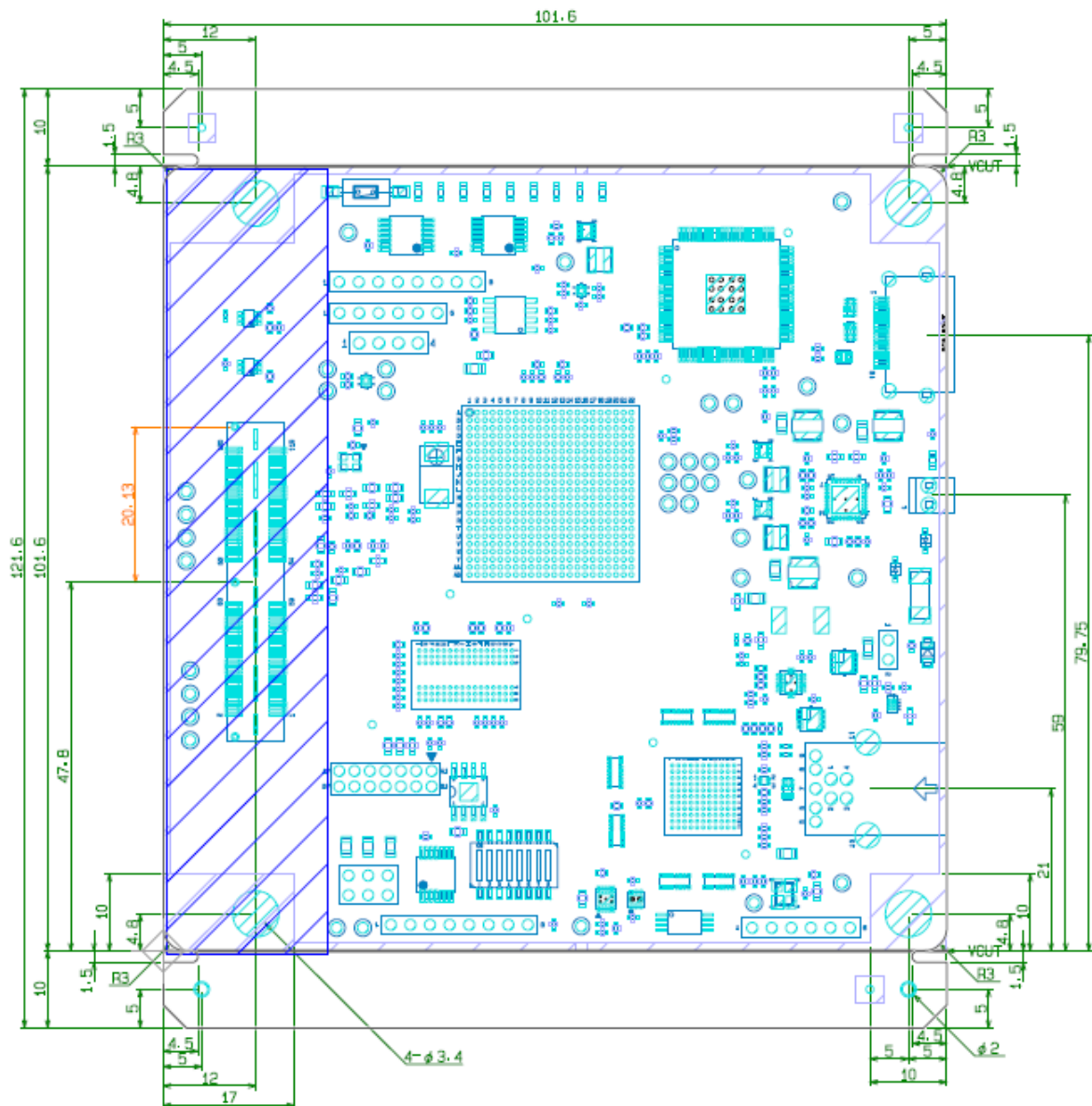
4. The Shape of SVO-06

The photo and drawing of the SVO-06 outline are shown below. (Same as SVM-06.)

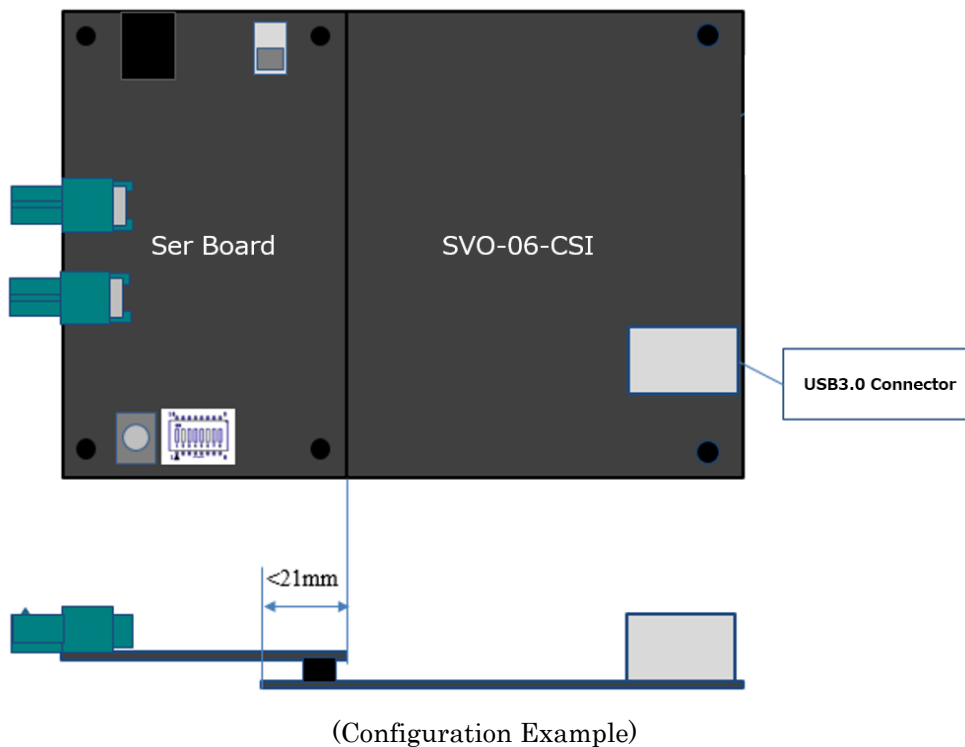
4.1. The Photo of SVO-06



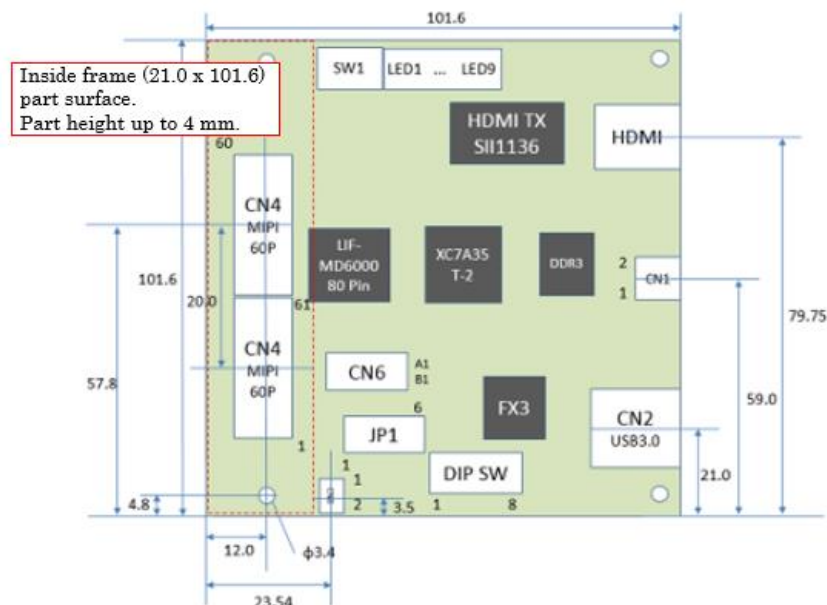
The drawing of SVO-06 is shown below. The actual board size does not include the 10mm parts to VCUT at each of the top and bottom. The size of this board is the same as our other SV series boards, 101.6 mm x 101.6 mm.



4.3. Dimensional Restriction of Connection Target Board



SVO-06 is used by connecting a target board like a serializer board to the connector CN4 as shown in the figure above. The target board is partially overlapped on SVO-06, but **the overlapped area between the two boards should be within 21 mm from the edge of SVO-06**. The area where the two boards can overlap is indicated by the red frame in the figure below. When you manufacture a target board with dimensions that exceed this frame, use a high connector or take other precautions for the board shape.



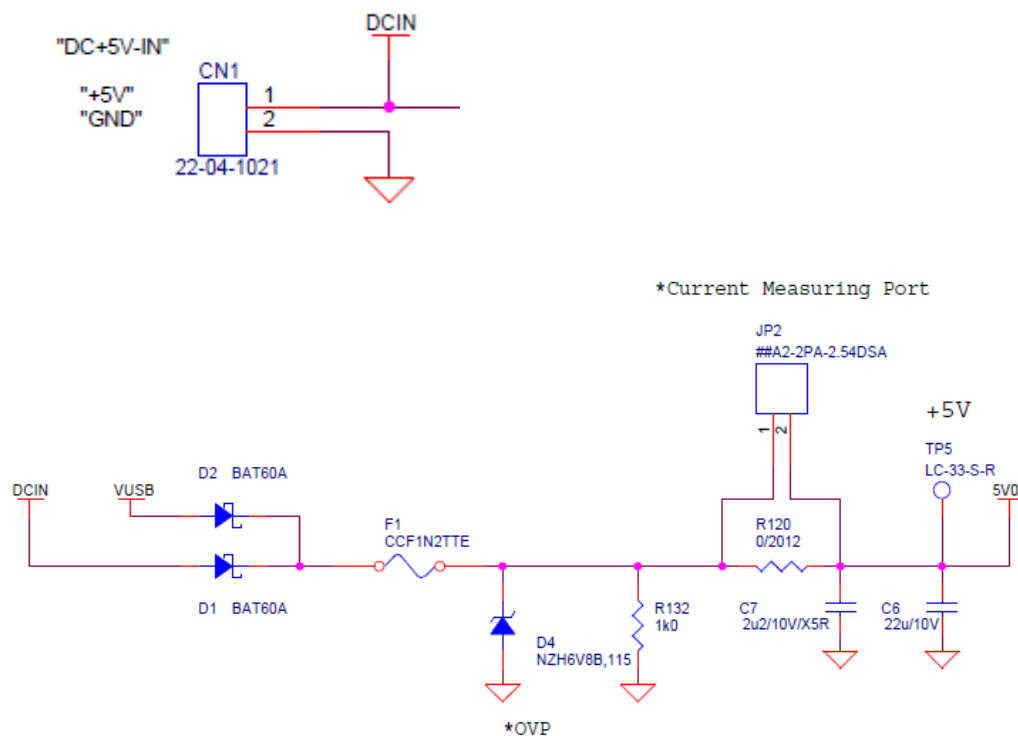
5. Connector Specification

In this chapter, we describe connector specifications that should be considered during normal use and connection to the target. Other connectors are described in the Appendix.

5.1. CN1: Sub Power Connector

This connector is used when the power is not satisfied or not supplied by USB bus power.

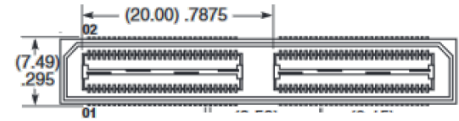
Connector		22-04-1021: Molex					
Pin #	Signal Name	Direction	Remarks	Pin #	Signal Name	Direction	Remarks
1	+5V	IN	DC5V Power input	2	GND	-	Power ground



- The +5V (DCIN) from CN1 and the +5V (VUSB) from USB connector are connected by diode OR as shown above and used as board internal power supply (5V0).

5.2. CN4: Target Connector

This connector is used to connect the target.



Basic Port

Connector		QSH-060-01-L-D-A: SAMTEC					
Pin #	Signal Name	Direction	Remarks	Pin #	Signal Name	Direction	Remarks
61	D1_N	OUT	MIPI Lane1 Output -	62	GPIO0	IO	GPIO 0
63	D1_P	OUT	MIPI Lane1 Output +	64	GPIO1	IO	GPIO 1
65	GND	-		66	GND	-	
67	D2_N	OUT	MIPI Lane3 Output -	68	GPIO2	IO	GPIO 2
69	D2_P	OUT	MIPI Lane3 Output +	70	GPIO3	IO	GPIO 3
71	GND	-		72	GND	-	
73	CLK_N	OUT	MIPI Clock Output -	74	GPIO4	IO	GPIO 4
75	CLK_P	OUT	MIPI Clock Output +	76	GPIO5	IO	GPIO 5
77	GND	-		78	GND	-	
79	D3_N	OUT	MIPI Lane2 Output -	80	GPIO6	IO	GPIO 6
81	D3_P	OUT	MIPI Lane2 Output +	82	GPIO7	IO	GPIO 7
83	GND	-		84	GND	-	
85	D4_N	OUT	MIPI Lane4 Output -	86	GPIO8	IO	GPIO 8
87	D4_P	OUT	MIPI Lane4 Output +	88	GPIO9	IO	GPIO 9
89	GND	-		90	GND	-	
91	SCL	OUT	I2C SCL Signal Line	92	GPIO10	IO	GPIO 10
93	SDA	IO	I2C SDA Signal Line	94	GPIO11	IO	GPIO 11

95	GND	-		96	GND	-	
97	GND	-		98	GND	-	
99	GND	-		100	GND	-	
101	GND	-		102	GND	-	
103	VSYNC	IN/OUT	VSYNC Input / Output (Reserved)	104	GPIO12	IO	GPIO 12
105	HSYNC	IN/OUT	HSYNC Input / Output (Reserved)	106	GPIO13	IO	GPIO 13
107	GND	-		108	GND	-	
109	CK	OUT	Clock Output (Reserved)	110	GPIO14	IO	GPIO 14
111	RST	OUT	Reset Output (L : Reset)	112	GPIO15	IO	GPIO 15
113	GND	-		114	GND	-	
115	VDDIO	POW	IO Power Output	116	1V2	POW	1.2V Power Output
117	3V3	POW	3.3V Power Output	118	3V3	POW	3.3V Power Output
119	GND	-		120	GND	-	
MP1	GND	-		MP2	GND	-	
MP3	GND	-		MP4	GND	-	

Extension port

Connector		QSH-060-01-L-D-A: SAMTEC					
Pin #	Signal Name	Direction	Description	Pin #	Signal Name	Direction	Description
1	D5_N	OUT	(Reserved)	2	NC		
3	D5_P	OUT	(Reserved)	4	NC		
5	GND	-		6	GND	-	
7	D7_N	OUT	(Reserved)	8	NC		
9	D7_P	OUT	(Reserved)	10	NC		
11	GND	-		12	GND	-	
13	CLK_N	OUT	(Reserved)	14	NC		

15	CLK_P	OUT	(Reserved)	16	NC		
17	GND	-		18	GND	-	
19	D6_N	OUT	(Reserved)	20	NC		
21	D6_P	OUT	(Reserved)	22	NC		
23	GND	-		24	GND	-	
25	D8_N	OUT	(Reserved)	26	NC		
27	D8_P	OUT	(Reserved)	28	NC		
29	GND	-		30	GND	-	
31	SCL	OUT	I2C SCL Signal Line	32	NC		
33	SDA	IO	I2C SDA Signal Line	34	NC		
35	GND	-		36	GND	-	
37	NC	-		38	GND	-	
39	NC	-		40	GND	-	
41	GND	-		42	GND	-	
43	5V0	POW	+5V Power Output	44	OD12	OUT	OD Output of GPIO12
45	5V0	POW	+5V Power Output	46	OD13	OUT	OD Output of GPIO13
47	GND	-		48	GND	-	
49	NC			50	EXTIN14	IN	Tolerant Input of GPIO14
51	NC			52	NC		
53	GND	-		54	GND	-	
55	VDDIO	POW	IO Power Output	56	5V0	POW	+5V Power Output
57	3V3	POW	3.3V Power Output	58	3V3	POW	3.3V Power Output
59	GND	-		60	GND	-	
MP1	GND	-		MP2	GND	-	
MP3	GND	-		MP4	GND	-	

- HSYNC and VSYNC pins are reserved for customization. There is no function in the standard version. (Hi-Z)
- GPIO pins are Hi-Z in the default state. The direction and level of each pin are set by the FPGA register.
- IO voltage of each single-ended port is determined by jumper JP1.
- SCL and SDA are connected to the I2C bus inside SVO-06 via level conversion IC.
- ODOUTn and EXTINn pins are 5V tolerant. Do not apply voltages above VDDIO to any other pins.

6. Detail of Each Part

6.1. SW1: Push Switch

No functions have been assigned yet.

6.2. SW2: DIP Switch

SW2 is 8-bit switch for setting the various modes of operation. You can set the following settings with this switch.

No. #	Name	Turns OFF	Turns ON
1	Board Number b3	b3=0	b3=1
2	(Reserved)	Normal Mode	
3	(Reserved)	Normal Mode	
4	Board Number b0	b0=0	b0=1
5	Board Number b1	b1=0	b1=1
6	Board Number b2	b2=0	b2=1
7	Operation Mode (At startup)	7: ON, 8: ON -> (Reserved)	
8		7: ON, 8: OFF -> Start in Updater Mode	
		7: OFF, 8: OFF -> (Reserved)	
		7: OFF, 8: ON -> Start in USB Mode	

- The board numbers b3-b0 are the numbers recognized by NVFilePlayer.

6.3. LED1-9: Operation State Indication

These LEDs indicate the operating state of SVO-06 or FPGA. These LEDs flash rapidly during the startup process and behave as shown below after normal startup. The following is the status in USB mode.

LED #	Description
1	Lights up when power supply to CN4 is enabled.
2	Always off.
3	Always off.
4	Always off.
5	Lights up when the pixel clock of the parallel signal generation block inside the FPGA is locked.
6	Blinks at a frequency that is one-third of the Vsync frequency. Always OFF when VC0 is not selected for output.

7	Always off.
8	Lights up when an image stored in the frame memory is being loaded for output to the target. The lighting status of this LED does not necessarily indicate image output to the target.
9	Lights up when a specific exception is detected inside the FPGA.

6.4. JP1: VDDIO Selection Jumper

JP1 is a jumper for selecting IO power supply (VDDIO) which is output from the SVO-06 for target device via the target connector CN4. It can be selected from 1.8 V, 2.5 V and 3.3 V.

VDDIO is intended to be used as an IO supply voltage for target devices. Also, GPIO0-15, CLK, RST, SCL, and SDA signal lines are input / output at the VDDIO power supply level.

In default, it is set to **3.3V**.

6.5. JP3: Configuration Setting Jumper

Normally, this jumper should be used in the **open position** (no jumper pins connected).

6.6. Guaranteed operating range

The operating temperature range of the IC on this board is 0-80°C. However, this operating temperature range does not take into account the heat generated by the device. When the device is operating, the IC die should be operated with the ambient temperature as low as possible to keep it within the 0-80°C range.

When the device operating above this temperature range or incorporating into a case, it is recommended that attaching a heat sink to the FPGA or using a fan.

7. Check Terminal

7.1. TP4: VDDIO Check Terminal (Red)

This is used to check the VDDIO voltage.

7.2. TP1, 3, 5, 6: Voltage Check Terminal (Red)

These are for checking each power supply voltage required for the operation of SVO-06. Normally, there is no need to check. Please do not use the power from these check terminals to supply power to external modules.

7.3. TP7-10: GND Check Terminal (Black)

Use it as a GND terminal.

8. Board Update

The firmware of this board is updated using "SVMUpdater" software. Please refer to the "SVMUpdater Software Manual" for details.

9. Applicable Version

Mode	FX3 Version	FPGA Version
USB mode	100 or later	1.00 or later (Custom code: UO)

10. Notes

For proper use of this board, be sure to follow the precautions below.

1. When you update the firmware / FPGA, set the DIP SW (SW2) to # 7 = ON, # 8 = OFF and use the update software (SVMUpdater) from a host PC.
2. When you connect and disconnect the target such as interface boards, be sure to turn off the power of this board.
3. Please use a power supply with sufficient current capacity to supply power to this board.
4. The contents of this document may be changed without notice.
5. Reprinting all or part of the contents of this document without permission is prohibited.
6. We are committed to the content of this document, but if you find any suspicious point, errors, or omissions, please contact us. E-mail: sv-support@net-vision.co.jp
7. Be sure to use NVFilePlayer / SVMUpdater software released after May 2024, when SVO-06-CSI was developed (NVFilePlayer: 1.3.5.6, SVMUpdater: 1.8.0.1 or later).
8. When inputting external signals to each signal line of connector CN4, be sure that the voltage does not exceed the VDDIO voltage of this board. Do not input external voltage when this board is not powered on, as this may result in a malfunction.
9. HDMI connector on this board cannot be used.

11. Appendix

11.1. CN2: USB3.0 Connector

CN2 is a connector that connects this board to a host PC. It can be connected via a commercially available USB 3.0 cable and is also a power supply connector for SVO-06.

Connector		1003-024-02000					
Pin #	Signal Name	Direction	Description	Pin #	Signal Name	Direction	Description
1	VBUS	IN	+5V Bus Power	2	D-	I/O	USB 2.0 Differential Pair-
3	D+	I/O	USB 2.0 Differential Pair+	4	GND	-	GND for Power
5	SSTX-	OUT	USB3.0 Transmission Differential Pair-	6	SSTX+	OUT	USB 3.0 Transmission Differential Pair+
7	GND DRAIN	-	GND for Signal	8	SSRX-	IN	USB 3.0 Receiver Differential Pair-
9	SSRX+	IN	USB 3.0 Receiver Differential Pair+				

11.2. CN6: FPGA-JTAG Connector

CN6 is a JTAG port used to write the SPI-ROM of FPGA bitstream or to debug the running FPGA. You don't need to use it normally.

*The direction is seen from the FPGA.

Connector		A3B-14PA-2DSA (71)					
Pin #	Signal Name	Direction	Description	Pin #	Signal Name	Direction	Description
1	GND	-		2	VREF	OUT	Reference Voltage (3.3V)
3	GND	-		4	TMS	IN	JTAG-TMS
5	GND	-		6	TCK	IN	JTAG-TCK
7	GND	-		8	TDO	OUT	JTAG-TDO
9	GND	-		10	TDI	IN	JTAG-TDI
11	GND	-		12	NC	-	(Disconnected)
13	GND	-		14	NC	-	(Disconnected)

- We do not guarantee the operation when you use it.