Parallel Generator Board

[SVP-01-G]

Hardware Specification

Rev.1.0

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	2023/04/06	New File (Translation of Japanese edition ver.1.3)	R.Sugo

Index

1.Overview

This document is a hardware specification of our **"SVP-01-G"**. This board converts video signals input via USB3.0 or DisplayPort to parallel interface. Output timing such as blanking area and frame rate can be set as desired for flexible camera emulation. This board has four modes; **USB mode**, **DisplayPort mode**, **UVC mode** and **Updater mode**.

In the USB mode, this board converts video signals input from USB3.0 into parallel signals. You use a video file (uncompressed .avi file or .frm file) stored on a PC. It is transferred to this board via USB3.0 using our software (NVFilePlayer or SVOGenerator), and then this board outputs it as parallel video signals. You can set video signal timing, pixel format, FSYNC synchronization, etc. from the software.

In the DisplayPort mode, this board converts video signals input from DisplayPort into parallel signals with resolution, timing and pixel format set by DIP SW or SPI-ROM and outputs them.

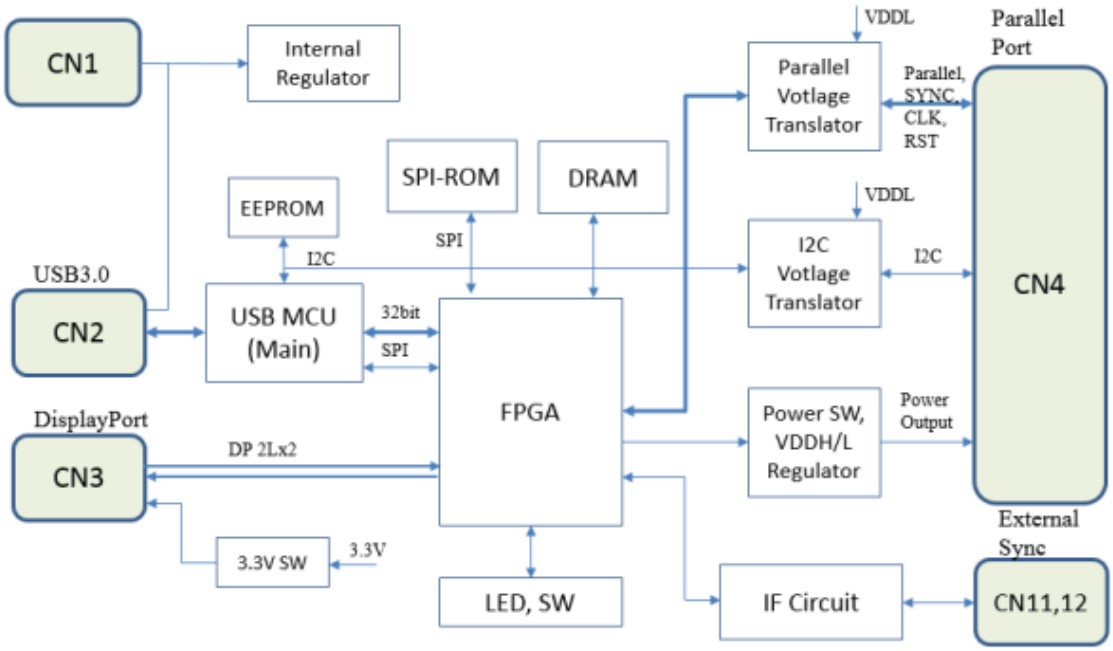
In the UVC mode, this board converts video signals input from DisplayPort into USB3.0. It is recognized from a PC as a UVC (USB Video Class) capture device.

In the Updater mode, you can update firmware of the microcontroller and FPGA of the board via USB. Be sure to start in the updater mode when you want to update this board.

You can switch each mode according to the startup state of the DIP SW (SW2) #7 and #8. Please see the table below for the switch setting of each mode.

#7	#8	Mode
OFF	ON	USB mode
OFF	OFF	DisplayPort mode
ON	ON	UVC mode
ON	OFF	Updater mode

1.1. Block Diagram



1.2. Specification

- Power: USB Bus Supply (External Power Supply can also be used)
  - Supply voltage: +5V (4.75-5.5V)
  - Operating current (typ): TBD
- Output Format (Via CN4, 5):
  - Parallel video signal (PCLK/VSYNC/HSYNC)
    - PCLK < 150MHz
    - Output Bit Width: 8bit / 16bit / 24bit / 32bit
    - Output Pixel Format: YUV4:2:2 (8bit), RGB24
    - IO Voltage (VDDL) Level: 1.8-3.3V
- Frame Memory: 256MB
- Output Resolution: Up to 8190 x 4095 pixel (4094x4095 at 8bit)
- USB Input: USB3.0 (NetVision own driver)
- USB Output: USB3.0 (USB Video Class)
- DisplayPort Input: DisplayPort 1.1a
  - Raw Bit Rate = 2.7Gbps/Lane x 2L (Throughput 4.3Gbps)
  - Input pixel format: RGB24 (24bpp RGB), YUV4:4:4(8bit), YUV4:2:2(8bit)
  - Dual-Mode (DP++): Not supported

  - HDCP: Not supported
- Power Output: IO voltage x1, Target voltage x2
- Serial Communication: I2C (max. 400kHz, device address 7bit)
  - IO voltage is the same as voltage level of the video signal (VDDL).
- Reset Signal Output
- Clock Signal Output
- FSYNC Signal Input
- GPIO Input/Output (video signal + GPIO = Up to 32bit)
  - 32bit can be used by mounting connector CN5.
- USB Device Name
  - UVC mode: “SVP-01G(UVC)”
  - If you assign a board ID, a number such as "(1)" is added to the end of the board name.

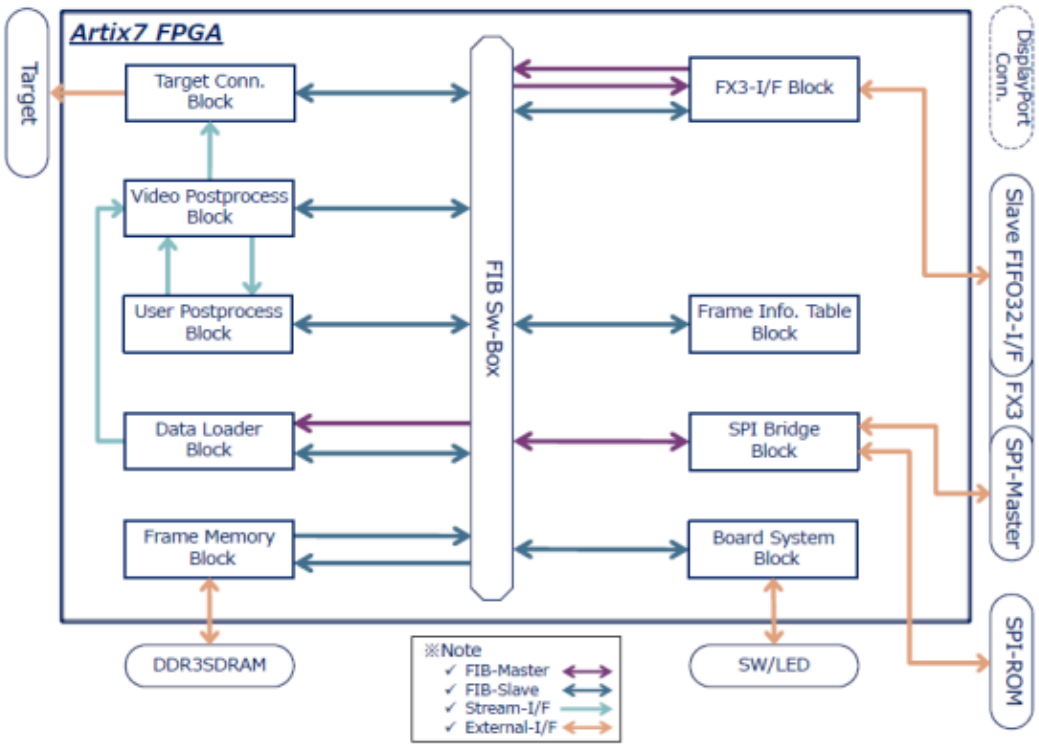
2. USB Mode Operation Details

This section describes USB mode. You use USB mode by booting this board with DIP SW set to #7: OFF and #8: ON.

2.1. USB Mode Specifications

- This board can convert uncompressed .avi files or .frm files saved on a PC to 8-32bit parallel video signals and output them.
- This board transfers videos in uncompressed format, so the image quality is not compromised. Therefore, it is ideal for evaluation tests and algorithm developments.
- This board supports Windows OS.
- You can download our video output software (NVFilePlayer, SVOGenerator) from our web page.
- It is possible to support output-timing-synchronization (FSYNC) with external signals.
- This board outputs uncompressed video data up to 3.2 Gbps (theoretical value) with high-speed transfer of USB3.0.
- There are 2 modes; one is that this board repeatedly outputs frames stored in DRAM, and another is that it transmits frames from a PC at any time.
- The target connection side is pin compatible with our old product SVO-03, so it is possible to use this board with the target that you have been using.
- You can also use the same software as SVO-03 for this board.
- This board can be used in stand-alone mode, outputting any pattern simply by turning on the power. We can provide the package including FPGA for the mode and Pattern Generator software. Please contact us for details.

2.2. FPGA Internal Block Diagram in USB Mode



2.3. USB Mode Setting

・IO voltage and output voltage setting

It is necessary to set the VDDL to the IO voltage of the image sensor or the conversion board before you connect your target device. Using the VDDH output and 3.3V output is possible, so if you want to use, please set them accordingly.

・DIP SW setting

If you connect multiple boards to one PC and output videos at the same time, you can distinguish boards by setting the board number recognized from the PC. The board number can specify with DIP SW.

・Initial settings from PC

The images can transfer to this board by connecting the PC via USB3.0 cable and using our software (NVFilePlayer or SVOGenerator). Please refer to software manuals for how to use the software and how to install the driver.

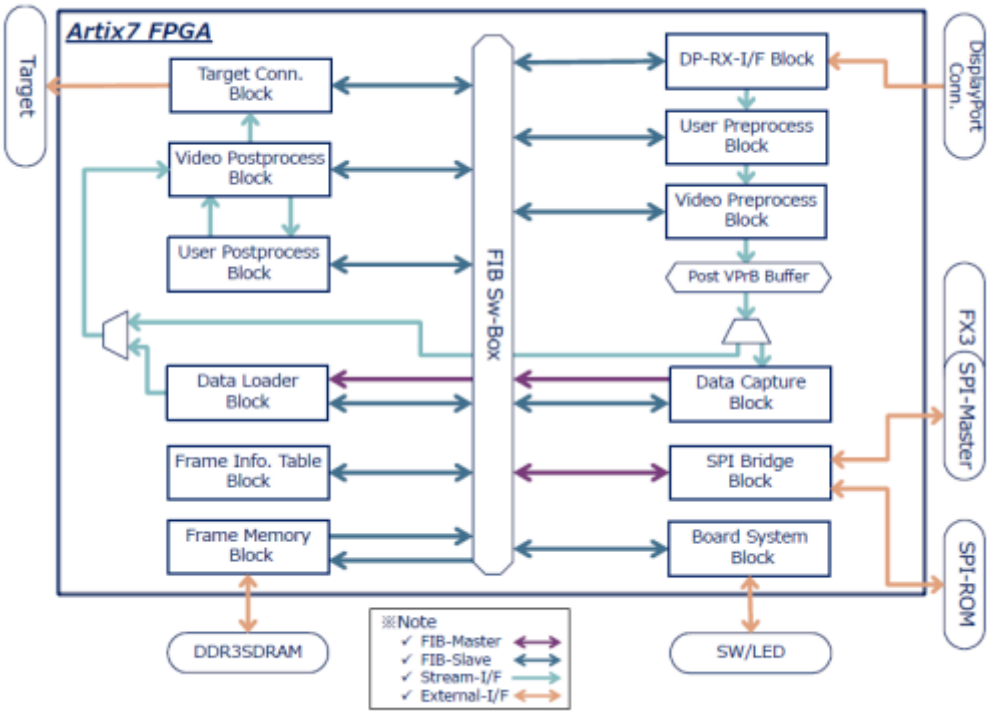
3. DisplayPort Mode Operation Details

This section describes DisplayPort mode. You can use DisplayPort mode by booting this board with DIP SW set to #7: OFF and #8: OFF.

3.1. DisplayPort Mode Specifications

- This board works as a DisplayPort receiver. It converts video signals input from the DisplayPort connector into parallel video signals.
- The output signal timing and the DisplayPort EDID can be set freely.
- You can download the software SVMCtl for setting of this board from our web page.
- The output format is stored in output timing data and it can be written to Flash ROM by using our software SVMCtl.
- If you don't write any output timing data, preset settings are applied (1080p or 720p set by DIP SW).
- The settings in SVMCtl are written to Flash ROM. Therefore, it can be operated with the settings only +5V power supply.
- This board can support output timing synchronization (FSYNC) with the external signals.
- This board supports YUV (4:2:2 8bit) and RGB (24bit) as standard input/output image format. This board do color conversion when the input pixel format is different from the output pixel format.
- The target connection side is pin compatible with our old product SVO-03, so it is possible to use this board with the target that you have been using.

3.2. FPGA Internal Block Diagram in DisplayPort Mode



3.3. Output Timing Data Preparing

If you use signals other than preset resolutions (1920x1080, 1280x720, 30fps / 60fps), you need to write output timing data and EDID file to the board.

Output timing data (.svo file) is created in software NVFilePlayer or SVOGenerator. First, you boot the board in USB mode (DIP SW #7 = OFF, #8 = ON) and open the software. Next, click "Device Setting" and set the timing parameter as same as the USB mode. And then you can write out .svo file with "SAVE SET".

Please refer to software manuals for details of operating "NVFilePlayer" and "SVOGenerator".

Alternatively, you can also use another software "TimingGenSVP01.exe" to create .svo files. In this case, you don't need to connect the board to a PC.

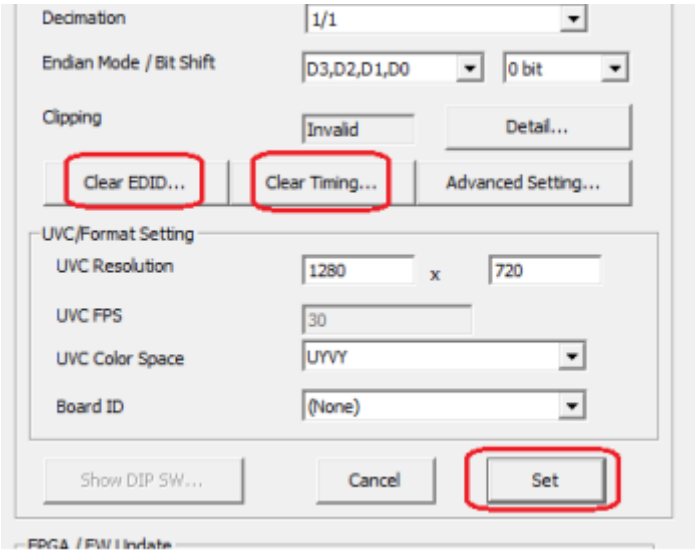
3.4. EDID File Preparing

This board works as a DisplayPort Sink (receiver), and sends EDID (Extended Display Identification Data) settings for notifying resolution and timing supported as the receiver to the DisplayPort Source (transmitter). If you write the output timing data, you need to set EDID with the same resolution as the output resolution. If you don't write the output timing data, the preset EDID is applied.

You need to prepare 256byte EDID file including Extended-EDID or 128byte binary file not including Extended-EDID. Please create it in a general EDID editor.

3.5. Procedure of data writing

You can write the timing data (.svo file) and the EDID file with SVMCtl. You boot this board in DisplayPort mode (DIP SW #7, #8 = OFF) and open SVMCtl, then click "SVM Setting..." button to call the setting screen.



If any timing data is written to the board in advance, "Clear Timing..." is displayed. Please click the button to clear the data.

If no output timing data is written, "Update Timing..." is displayed, so click the button and specify the timing data (.svo file).

Similarly, you can clear EDID file with "Clear EDID..." and set EDID file with "Update EDID...".

After completing these steps, click "Set" to write the data to SPI-ROM. And the setting data will be reflected when you reboot the board.

4. UVC Mode Operation Details

This section describes UVC mode. You can use UVC mode by booting this board with DIP SW set to #7: ON and #8: ON.

4.1. UVC Mode Specifications

- This board works as a DisplayPort receiver in the UVC mode. It sends video signals input from the DisplayPort connector as a UVC (USB Video Class) to a PC.
- The DisplayPort EDID can be set freely. It is same as DisplayPort mode.
- If you don't write EDID data, the preset resolution (1080p or 720p, selected by DIP SW) is applied.
- You can download our utility software SVMCtl for settings from our web page.
- This board supports YUV (4:2:2 8bit) and RGB (24bit) as standard input/output image format. This board do color conversion when the input pixel format is different from the output pixel format.

4.2. UVC Mode Setting

1. Input/Output resolution settings

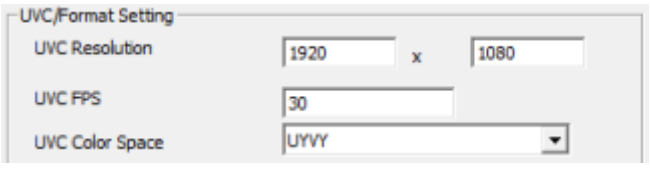
If you want the board to run at a preset resolution (720p, 1080p), set it with DIP SW. Please refer to "6.3. SW2: DIP Switch" for details.

2. Initial settings

It is necessary to make initial settings such as resolution and pixel format from a PC. You can set these settings with our software "SVMCtl". Please refer to the SVMCtl Software Manual for details.

If you want the board to run other than the preset resolutions, prepare an EDID file and write it to the board. This procedure is the same as for DisplayPort mode. You do not need to write timing data.

- Set the UVC Resolution and the UVC FPS as same as the EDID settings.
- Set the UVC Color Space to the pixel format that you want to output to the PC. It supports "UYVY" and "RGB24".



- Set the clipping function to OFF.
- If you do not write the EDID, settings with DIP SW are applied. In this case, UVC settings are not used.
- SVMCtl may be updated from time to time. You can download the latest version from our web page.
- This board is recognized as a capture device named "SVP-01G (UVC)" from the PC.
- If you assign a board ID with SVMCtl, the ID number is added to the end of the board name.

5. Shape of the SVP-01-G Board

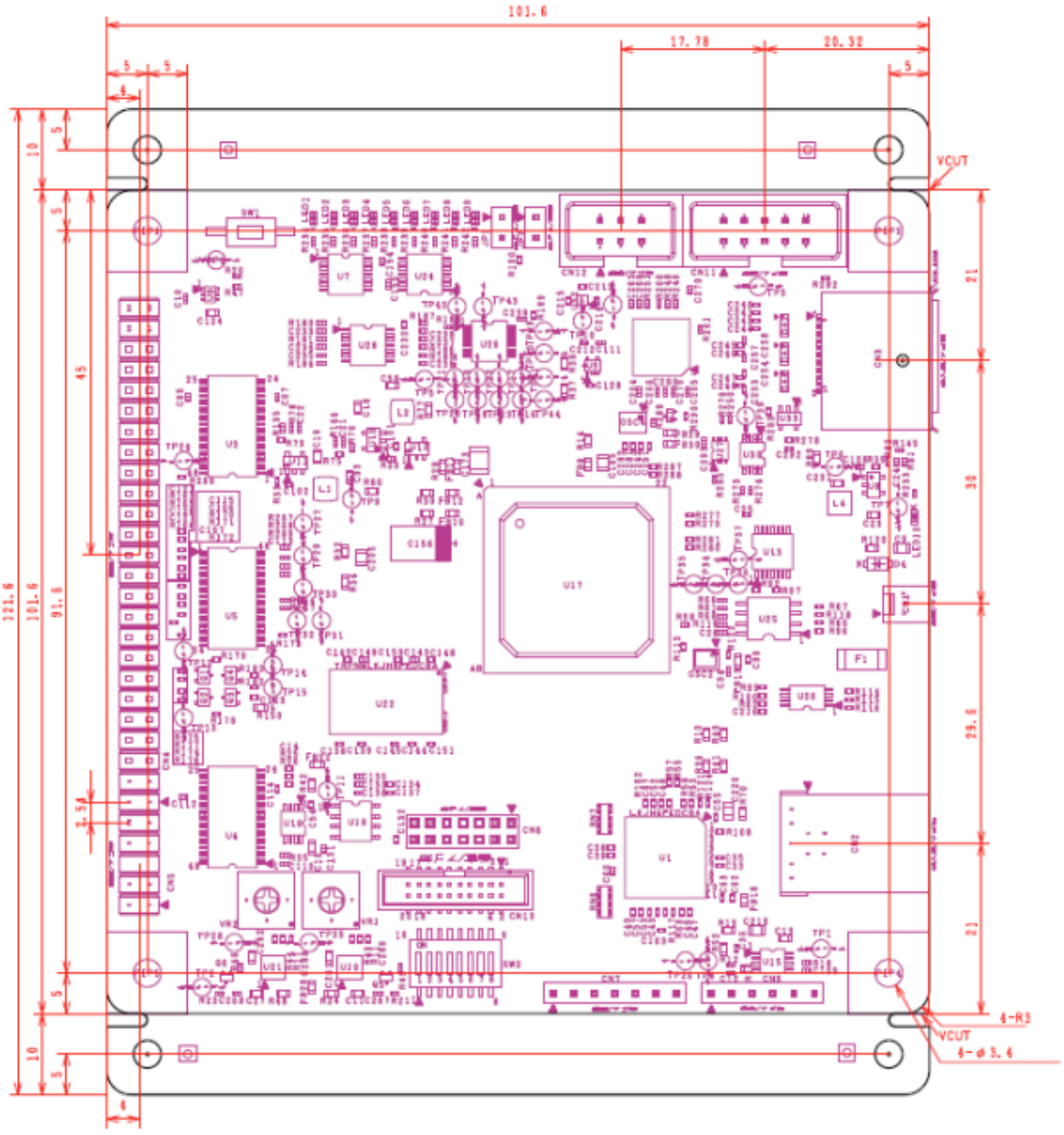
The photo and the Drawing of this board are shown below.

5.1. Photo of the Board

- Depending on lots, the mounted states of the parts may be different.
- SVP-01-G and SVP-01-U are same boards, but the firmware is different. Please refer to a label on the back of the board for board type.

5.2. Drawing

The top and bottom 10mm are breakaway PCBs. They don't attach the board.



6. Connector Specification

This chapter describes the connector specifications that should be considered in normal use.

6.1. Connector List

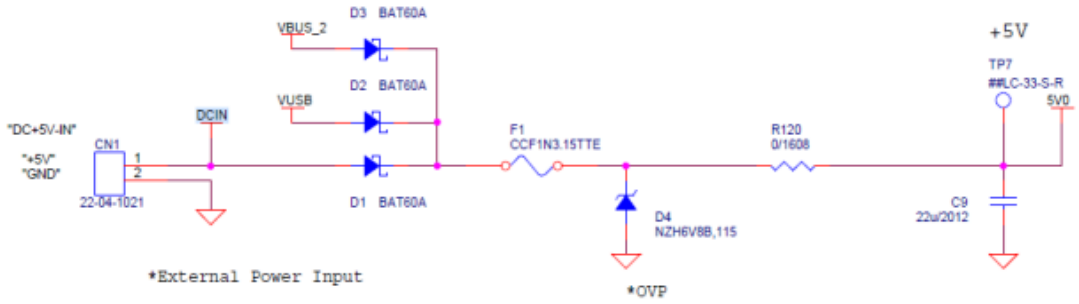
CN#	Mounted State	Model number	Function
CN1		22-04-1021	Sub power connector
CN2		1003-024-02000	USB3.0 type-B connector
CN3		0472720001	DisplayPort connector
CN4		PRPC025DAAN-RC	Parallel signal input/output (1-50P)
CN5	Un-mounted	PRPC005DAAN-RC	Parallel signal input/output (51-60P)
CN6		0877581416	JTAG connector
CN7	Un-mounted	A2-7PA-2.54DSA	(For debug)
CN9	Un-mounted	A2-6PA-2.54DSA	(For debug)
CN10	Un-mounted	A2-6PA-2.54DSA	(For debug)
CN11	Un-mounted	87834-1019	For synchronous wiring connector (5x2)
CN12	Un-mounted	87834-0619	For synchronous wiring connector (3x2)
CN13		3220-20-0300-00	For shipping check connector

- Mounted states are standard specifications of SVP-01-G.
- CN6-CN13 are not used normally.
- You need to mount CN5 when you want to extend the bit width of parallel signals.

6.2. CN1: Sub Power Connector

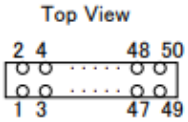
This connector is used when USB bus power cannot meet power capacity.

Used connector		22-04-1021: Molex					
Pin number	Signal name	Direction	Note	Pin number	Signal name	Direction	Note
1	+5V	IN	DC5V power input	2	GND	-	Power ground



- Power input of CN1, VBUS (VUSB) of CN2, and VBUS (VBUS_2) of CN3 are connected by diode OR as shown in above figure.
- Input voltage range is 4.75 ~ 5.5V.

6.3. CN4: Target Connection Connector A



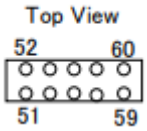
This connector is a 2.54mm pitch pin header for connecting a target image sensor. It can be connected with a general pin socket or IDC cable. By using CN4 and CN5 in combination, you can connect image sensors with bit width of 24-32 bits.

Used connector		PRPC025DAAN-RC					
Pin number	Signal name	Direction	Note	Pin number	Signal name	Direction	Note
1	VDDL	OUT	IO voltage level output (1.8-3.3V)	2	GND	-	-
3	P0	OUT	General purpose output port 0 / Pixel_DATA16	4	GND	-	-
5	P1	OUT	General purpose output port 1 / DE output (8-16bit) / Pixel_DATA17	6	GND	-	-
7	P2	OUT	General purpose output port 2/ Pixel_DATA18	8	GND	-	-
9	P3	IN / OUT	General purpose input port 0 / Pixel_DATA24	10	GND	-	-
11	P4	IN / OUT	General purpose input port 1 / DE output (24bit) / Pixel_DATA25	12	HSYNC	OUT	Horizontal synchronization output
13	VSYNC	OUT	Vertical synchronization output	14	XRST	OUT	Reset signal output
15	VDDH	OUT	Target power output (1.2 - 3.6V can be set)	16	GND	-	-
17	SDA	IO	I2C_DATA	18	GND	-	-

Used connector		PRPC025DAAN-RC					
Pin number	Signal name	Direction	Note	Pin number	Signal name	Direction	Note
19	SCL	IO	I2C_CLK	20	GND	-	-
21	DCK	OUT	Pixel_CLK (Pixel clock)	22	GND	-	-
23	Y0	OUT	Pixel_DATA0	24	GND	-	-
25	Y1	OUT	Pixel_DATA1	26	GND	-	-
27	Y2	OUT	Pixel_DATA2	28	GND	-	-
29	Y3	OUT	Pixel_DATA3	30	GND	-	-
31	Y4	OUT	Pixel_DATA4	32	GND	-	-
33	Y5	OUT	Pixel_DATA5	34	GND	-	-
35	Y6	OUT	Pixel_DATA6	36	GND	-	-
37	Y7	OUT	Pixel_DATA7	38	GND	-	-
39	CLKOUT	OUT	Target drive clock	40	GND	-	-
41	Y8	OUT	Pixel_DATA8	42	Y9	OUT	Pixel_DATA9
43	Y10	OUT	Pixel_DATA10	44	Y11	OUT	Pixel_DATA11
45	Y12	OUT	Pixel_DATA12	46	Y13	OUT	Pixel_DATA13
47	Y14	OUT	Pixel_DATA14	48	Y15	OUT	Pixel_DATA15
49	3V3	OUT	3.3V output	50	P5	IN / OUT	General purpose input port 2 / Pixel_DATA26

6.4. CN5: Target Connection Connector B

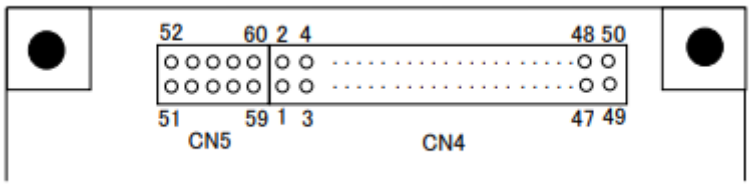
This is a connector for connecting a target.



Used connector		PRPC005DAAN-RC					
Pin number	Signal name	Direction	Note	Pin number	Signal name	Direction	Note
51	P6	IN / OUT	General purpose input port 3 / Pixel_DATA27	52	P7	IN / OUT	General purpose input port 4 / Pixel_DATA28
53	P8	IN / OUT	General purpose input port 5 / Pixel_DATA29	54	P9	IN / OUT	General purpose input port 6 / Pixel_DATA30
55	P10	IN / OUT	General purpose input port 7 / Pixel_DATA31	56	P11	OUT	General purpose output port 3 / Pixel_DATA19
57	P12	OUT	General purpose output port 4 / Pixel_DATA20	58	P13	OUT	General purpose output port 5 / Pixel_DATA21
59	P14	OUT	General purpose output port 6 / Pixel_DATA22	60	P15	OUT	General purpose output port 7 / Pixel_DATA23

- CN5 is optional, and is not mounted as standard.
- The input / output directions of Pixel_DATA [31:24] are changed depending on output bit width setting.

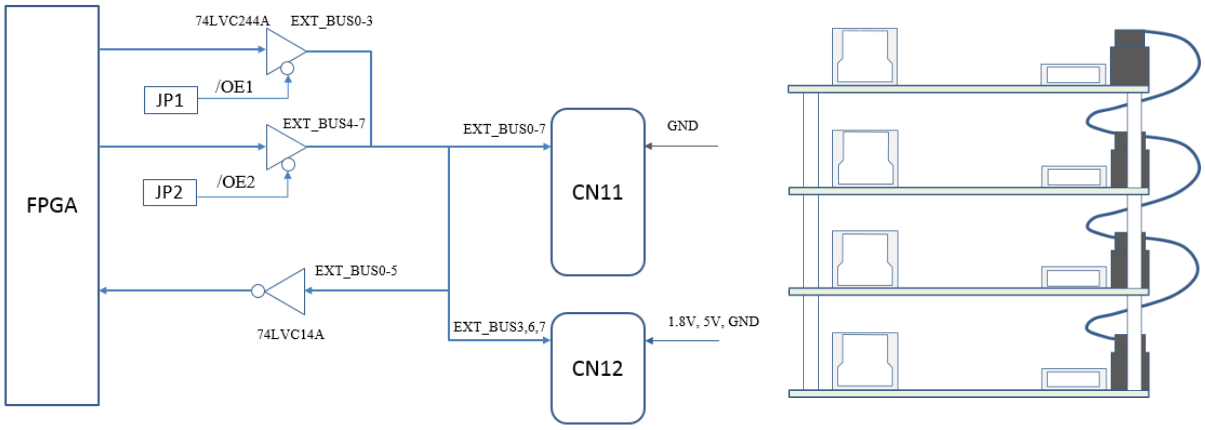
6.5. Positional Relationship Between CN4 and CN5



- You can use CN4 and CN5 in combination as a 60pin-header.

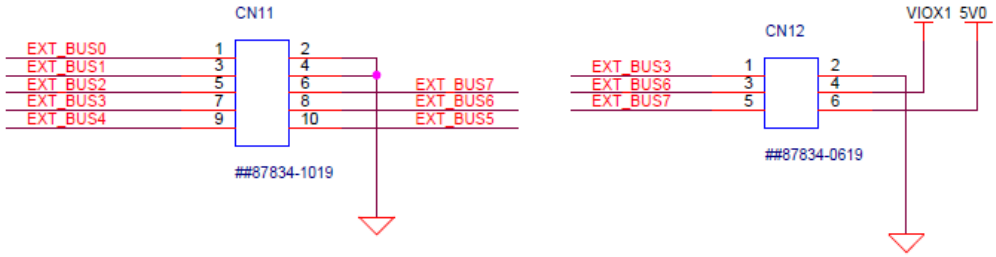
6.6. CN11, CN12: Connectors for Synchronous Wiring

CN11 and CN12 are connectors for synchronous wiring board to board. It is possible to wire with 2.54mm pitch IDC connector. You can use custom functions such as synchronous capturing and time stamping by using these connectors to connect multiple SV series boards. These connectors aren't used in the standard specification. (It will be supported in the future.)



(Block Diagram)

When JP1 is shorted, EXT_BUS0-3 signal line will be output. When JP2 is shorted, EXT_BUS4-7 signal line will be output.



(Pin Assignment)

6.7. Input Data Configuration

When you output images with YUV or RGB24, connect the wires according to the table below.

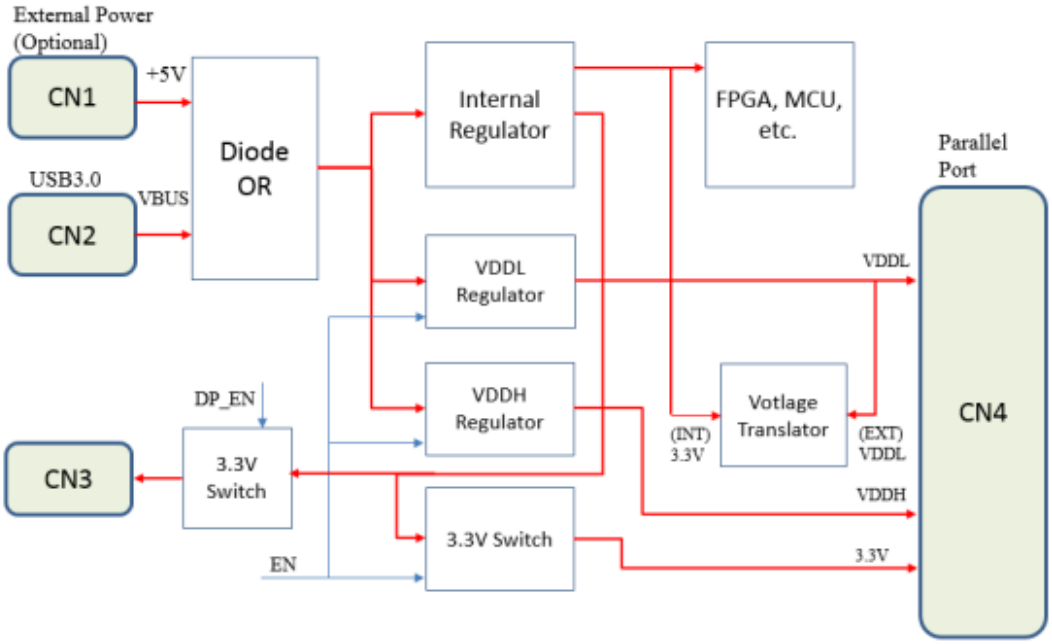
Format	YUV4:2:2			RGB24
Bit Width	8bit (UYVY/YUY2)	16bit (UYVY)	32bit (UYVY)	24bit
Pixel_DATA [31:24]	-	-	V	-
Pixel_DATA [23:16]	-	-	Y	R
Pixel_DATA [15:8]	-	U, V	U	B
Pixel_DATA [7:0]	Y, U, V	Y	Y	G

- The polarity of the VS, HS, and clock signals can be set freely.

7. Details of Each Part

7.1. Power Supply System

The power supply system of this board is shown below. The board power supply can be operated by USB power supply or external +5V. Some of internal regulators are output to CN4, and your connected device can also operate with USB power supply.



7.2. SW1: Push Switch

SW1 is a switch for controlling reset output signal line and sending initial settings to the I2C bus. In the DisplayPort mode, you can change SW1 function with SVMCtl. This switch is not used in USB mode normally. Please refer to the SVMCtl software manual for more information.

7.3. SW2: DIP Switch

This is an 8bit switch for setting various operating modes. You can set following items depending on the mode.

7.3.1. USB Mode

Number	Item	OFF	ON
1	Board number b3		
2	(Reserved)	Standard operation	
3	(Reserved)	Standard operation	
4	Board number b0		
5	Board number b1		
6	Board number b2		
7	Operation mode setting (at start up)	7: ON, 8: OFF: Updater mode 7: OFF, 8: ON: USB mode 7: OFF, 8: OFF: DisplayPort mode 7: ON, 8: ON: UVC mode	
8			

The SW#1, #6-4 (board number b3-b0) indicate the board number recognized by NVFilePlayer / SVOGenerator.

7.3.2 DisplayPort Mode

Number	Item	OFF	ON
1	Camera output bit width setting 1 (at #3 = OFF)	8bit x 2 CLK (YUV)	16bit x 1 CLK (YUV) or 24bit x 1 CLK (RGB)
2	External synchronization mode (when timing data is written)	Free run operation	External synchronization mode
	Frame rate (when timing data is not written)	60FPS (30FPS at PCLK > 150MHz)	30FPS fixed
3	Camera output bit width setting 2	(Following DIP SW #1)	32bit x 1/2 CLK (YUV)
4	Sort setting (only YUV 8bit x 2CLK)	UYVY format	YUY2 format
5	Image input / output format setting	ON: RGB888 output OFF: YUV422 8bit output	
6	Image input / output resolution setting	ON: 720p (1280 x 720) OFF: 1080p (1920 x 1080)	
7	Operation mode setting (at startup)	7: ON, 8: OFF: Updater mode 7: OFF, 8: ON: USB mode 7: OFF, 8: OFF: DisplayPort mode 7: ON, 8: ON: UVC mode	
8			

- When you use RGB output, set the SW #4 = OFF.
- If the output timing data is written in the board, the resolution and frame rate settings with DIP SW are ignored.
- The external sync function is enabled when all three of the following are set: timing data is written, external sync is set, and DIP SW #2 = ON.

7.3.3 UVC Mode

Number	Item	OFF	ON
1	(Reserved)	Standard operation	
2	Specification of frame rate	60FPS	30FPS
3	(Reserved)	Standard operation	
4	(Reserved)	Standard operation	
5	Image output format setting	ON: RGB888 output OFF: YUV422 8-bit output	
6	Image input / output resolution setting	ON: 720p (1280 x 720) OFF: 1080p (1920 x 1080)	
7	Operation mode setting (at start up)	7: ON, 8: OFF: Updater mode 7: OFF, 8: ON: USB mode 7: OFF, 8: OFF: DisplayPort mode 7: ON, 8: ON: UVC mode	
8			

- If EDID is written in the board, the resolution and frame rate settings with DIP SW are ignored.

7.4. LED1-10: Operating Status Indication

These LEDs display the operating status of the board and FPGA.

LED#	Explanation
1	When this is lit, it indicates that the board is supplying power to the target. This is a red LED.
2	This flashes at the cycle of the V-Sync synchronization signals to the target divided by 3. When the output videos are 30 fps, it repeats flashing 5 times per second.
3	<Reserved>
4	<Reserved>
5	<Reserved>
6	<Reserved>
7	This flashes at the cycle of the V-Sync synchronization signals to the target divided by 3 when the internal integrated video synchronization signal source is active.
8	<Reserved>

9	(USB mode) <Reserved> (DisplayPort mode) This flashes at the cycle of the V-Sync synchronization signals from the DisplayPort receiver divided by 3.
10	When this is lit, it indicates that the power is supplied to the board.

- The LEDs marked as "Reserved" will be assigned for future functions. In the current version, the lighting states change depending on the board inside status.
- While the I2C setting is being sent, the LED1-8 flash at high speed.
- If the license key is not written in the board, the LEDs 1-8 light up slowly and sequentially.
- During the DisplayPort connection process in the DisplayPort mode, the LEDs 1-6 light up in sequence. After the process is complete, they will be returned to the original states.
- If the board stops working due to a USB error, all LEDs will flash slowly at the same time.

7.5. VR1, VR2: VDDH and VDDL variable resistors for Adjusting

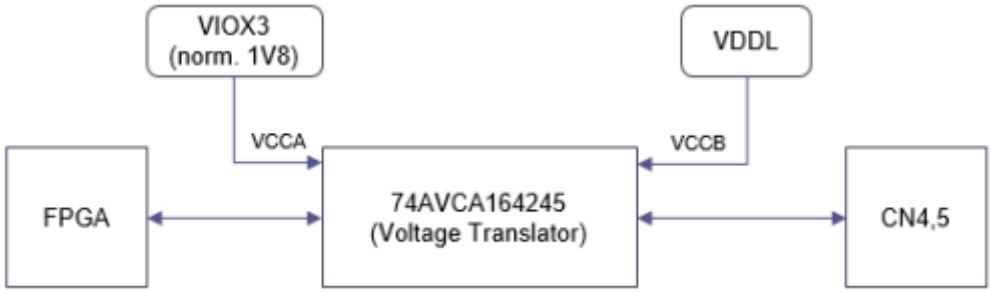
These are variable resistors that adjust the power supply for the target device generated by SVP-01-G. You can adjust the VDDL in the range of 1.8V - 3.3V and the VDDH in the one of 1.2V - 3.6V.

The VDDL is connected to the translator IC. The voltage levels of parallel video output signals and general inputs / outputs are same as VDDL voltage. The VDDL must be set according to the target.

On the other hand, the VDDH only connects to the connector and is not used inside the board. It can be used as the power supply for the target.

The VDDL and VDDH are set to 3.3 V at the time of shipment. You should adjust them according to your target before using.

7.6. CN4,5 Input/Output Circuit Schematic Diagram



- The IO voltages of each single ended IO pins of CN4, CN5 are determined by the VDDL voltage.

7.7. The Operating Temperature

The operating temperature range of the ICs on this board is 0-80℃. However, this value is not considered about the heat generation of the device. Therefore, to allow the IC die to operate in the 0-80°C range, the ambient temperature (the operating temperature range) should be 0-36°C in USB mode and DisplayPort mode when the device is operating. We have confirmed that it works even at temperatures higher than this (60°C), but we cannot guarantee it.

If you want to operate it in a higher temperature or if you put it into a case, it is recommended to attach a suitable heat sink to the FPGA or to cool it with a fan.

For reference, under the conditions of that a heat sink LPD25-15B (25x25x15mm) attached to the FPGA and natural air cooling in an open space, the maximum operating temperature calculated in the same way is 49°C in USB mode and DisplayPort mode. (Measured in our in-house environment)

8. Applicable Version

This document supports the following versions.

Mode	FX3 Version	FPGA Version
Updater mode	After 101	After 0.20
USB mode	After 100	After 1.00
DisplayPort mode	After 123	After 1.15

UVC mode	After 123	After 1.15
SVMCtl	After v1.5.0.0	
SVMUpdater	After v1.7.3.0	

9. Precaution

When you use this board, please observe the following precautions.

1. When updating the firmware / FPGA, set the DIP SW (SW2) #7 = ON, #8 = OFF and use the update software (SVMUpdater) on a PC.
2. Please turn off this board when you connect and disconnect your target such as an interface board.
3. When you use an interface board or connect a device to the DisplayPort, you should consider the current consumption for them.
   Therefore, please use a power supply with sufficient power and current capacity for this board.
4. We may change the contents of this document without advance notice.
5. If you notice any suspicious points, errors, omissions, etc., please contact us.
   E-mail: sv-support@net-vision.co.jp.
6. Be sure to use SVMCtl / SVMUpdater software released after the development of SVP-01-G (SVMCtl: v1.4.7.2 or later, SVMUpdater: v1.7.3.0 or later). If you use an older version of the software to update or set this board, the software may not recognize this board and may not work properly.