USB3.0 Video Capture Board
[SVI-09]
Hardware Specification

Rev.1.1

NetVision Corporation

Update History

Revision	Date	Note	
1.0	9 Jan. 2020	New File（Equivalent to Japanese version 2.1）	S. Usuba
1.1	28 Aug. 2020	・Changed “SVI compatible mode” to “Vendor mode” ・Added UVC mode ・Deleted descriptions or figures about Rev.1 and added about Rev.2 ・Corrected the description about Vendor mode, about LEDs, and some mistakes（Equivalent to Japanese version 2.8）	H. Suzuki

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1. Overview

This document is a hardware specification of the board **SVI-09** for capturing video signals output from the image sensor with USB 3.0 connection. SVI-09 has 2 mode types; **Vendor mode** and **UVC mode**.

Vendor mode is compatible with SVI-06 (old product) and works with vendor class drivers. A major feature of Vendor mode is that it can follow up and capture even if the image size changes during capture.

UVC mode, on the other hand, operates as a USB Video Class compliant video capture device, and you can use existing libraries and software to evaluate image sensors and develop algorithms in various OS.

Vendor mode and UVC mode can be switched with the DIP switch (SW2) #8 on the board. When #8 is on, it operates as vendor mode, and when #8 is off, it operates as UVC mode. Both modes support uncompressed video transfer at 1920x1080 60FPS or higher.

1.1. Specifications

- Power : USB Bus Supply（external power supply input available）/ +5V 0.7A typ.
- Input format (via CN 4,5):
  - Parallel video signal（Support PCLK/VSYNC/HSYNC; Embedded Sync (BT.656)）
  - Support sensors of PCLK 150 MHz or less
  - Input Bit Width: 8bit / 16bit / 24bit / 32bit
- Input format (via CN3): * Optional support
  - Parallel video signal（Support PCLK/VSYNC/HSYNC; Embedded Sync (BT.656)）
  - LVDS signal (max. 12 Data Lanes + 2 Clock Lanes)
  - MIPI signal (max. 4 Lanes x 2ch)
- Input resolution: max. 8191x8191 pix.
- Output: USB3.0 (USB Video Class or Vender driver)
- FPGA: Artix7 - XC7A35T-1FGG484C

2. Operation Details in Vendor mode

This chapter describes **Vendor mode**.

2.1. Main Functions and Features of Vendor mode

・ Vendor mode is compatible with SVI-06 (older product) and works with vendor class drivers.

・ It operates using the API and driver provided by our company.

・ Supports parallel input from CN4/5.

・ Supports two modes: monitoring mode and recording mode.

・ Supports uncompressed video transfer of 1920x1080 60FPS or higher.

・ Supports I2C communication.

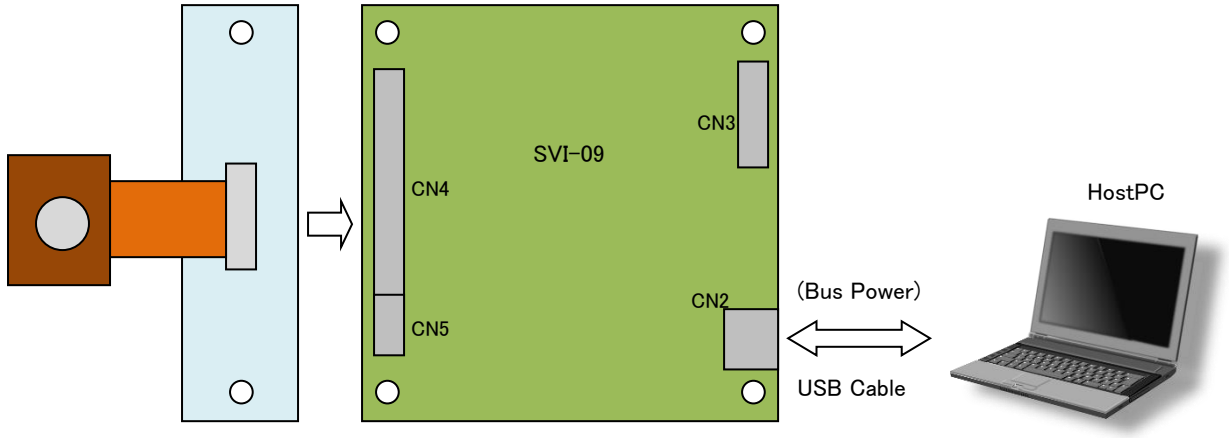
・ Has a function to regularly notify information to the host PC

・ Supports 8bit (YUV, 4:2:2), 8bit (RGB, 5:6:5), 16bit (YUV, 4:2:2), 16bit (RGB, 5:6:5), 8bit (RAW), 10bit (RAW), 12bit (RAW) as image data from camera module.

・ By equipped with an 8-bit general-purpose output port and an 8-bit general-purpose input port, settings on the evaluation board and status reading are possible.

・ By installing the PLL built-in clock generator for the image CLK in the FPGA, the system clock to the camera module can be changed arbitrarily.

2.2. Connection Example



2.3. Setting Procedure in Vendor mode

The necessary settings are listed below.

・Setting of target side power supply voltage (VDDL)

Before connecting the target device, it is necessary to adjust VDDL to the IO voltage of the image sensor or conversion board. The default is set to 3.3V.

・The initial value of the master clock to the target is 54MHz. Unlike SVI-06, there is no clock generator on the board, so it can change the setting from the PC application after startup.

・DIP SW setting

It is necessary to set the DIP SW for setting such as dividing the master clock output to the target device, setting the camera power OFF at startup, specifying the board number. For details, refer to the section 7.2.

・Initial setting from PC

It is necessary to perform initial setting such as pixel format from our application or an application using our API.

When you use our application, you use the software "SVImon" contained in the CD. For the usage of SVImon, refer to "SVI Software Manual".

3. Operation Details in UVC mode

This chapter describes **UVC mode**.

3.1. Main Functions and Features of UVC mode

・ It is USB Video Class (UVC) compliant and can be used just like a standard USB-connected Web-camera.
・ It works without a driver, and you can use various libraries such as DirectShow, OpenCV and ROS.
・ It supports Windows / Ubuntu (Linux) OS.
・ It supports I2C transfer by the Extension Unit and multi-channel capture with multiple units.
・ Dedicated DirectShow capture software (NVCap) is included on the attached CD.
・ It can capture uncompressed video data of up to 3.2 Gbps (theoretical value) by USB 3.0 high speed transmission.

3.2. Connection Example

Same as section 2.2.

3.3. Setting Procedure in UVC mode

In UVC mode, when you use the board the first time, you need to make the initial settings according to the specifications of the image sensor. If this setting is different from the specifications of the image sensor, the board cannot capture properly.

The necessary settings are listed below.

・Setting of target side power supply voltage (VDDL)

Before connecting the target device, it is necessary to adjust VDDL to the IO voltage of the image sensor or conversion board. The default is set to 3.3V.

・DIP SW setting

It is necessary to set the DIP SW according to bit width of target device. For details, refer to the section 7.2.

・Initial setting from PC

It is necessary to do initial setting such as resolution or pixel format from your PC.

You can set them using the SVMCtl software included in the CD. For details on SVMCtl operation, refer to SVMCtl Software Manual.

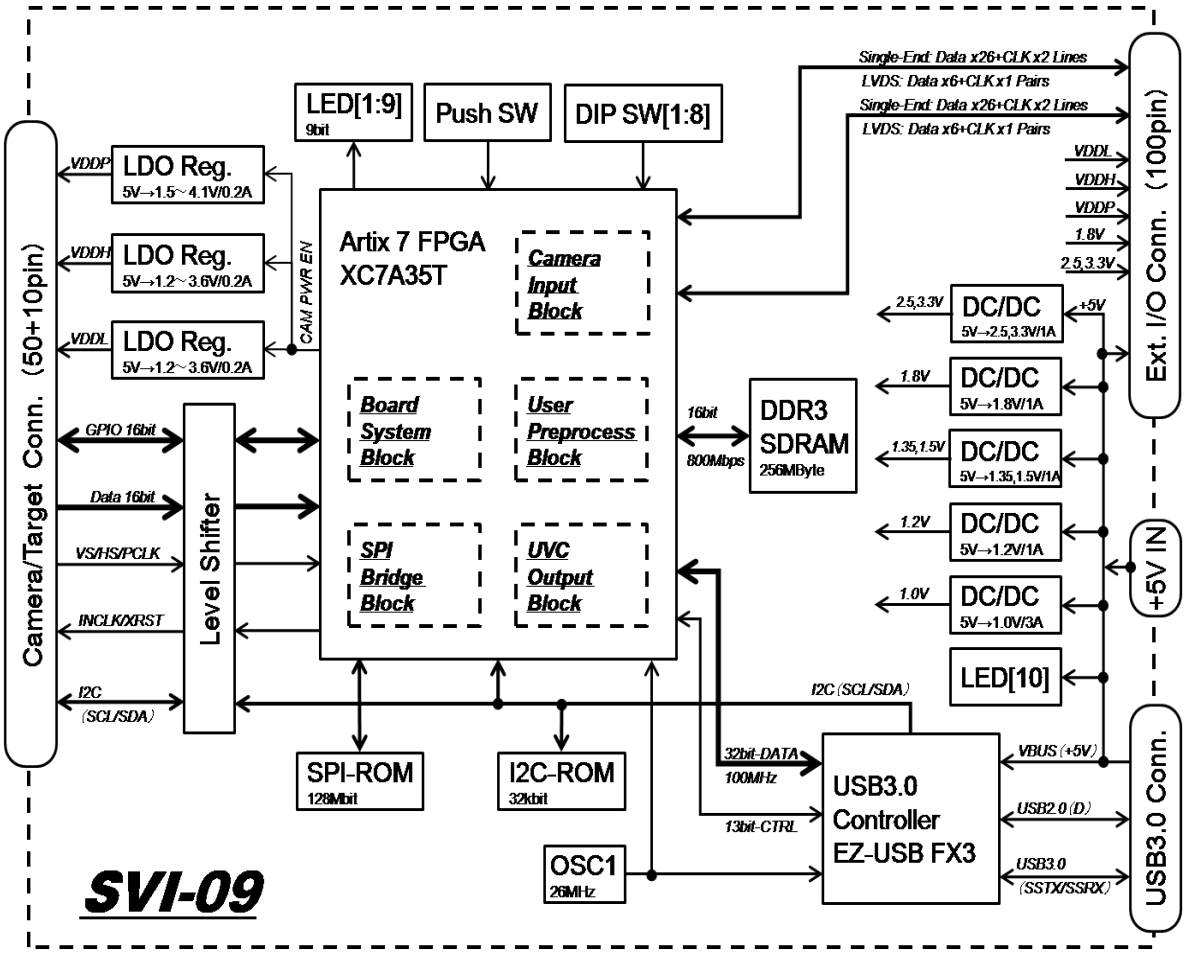
The default setting is below.

Pixel Clock: Sample at Rise
H-Sync Signal: Low Active
V-Sync Signal: Low Active
Resolution: 1280x720
Frame Rate: 30 FPS
Color Space: UYVY

- SVMCtl may be updated needly. You can download the latest version from our web page.

4. Block Diagram of SVI-09

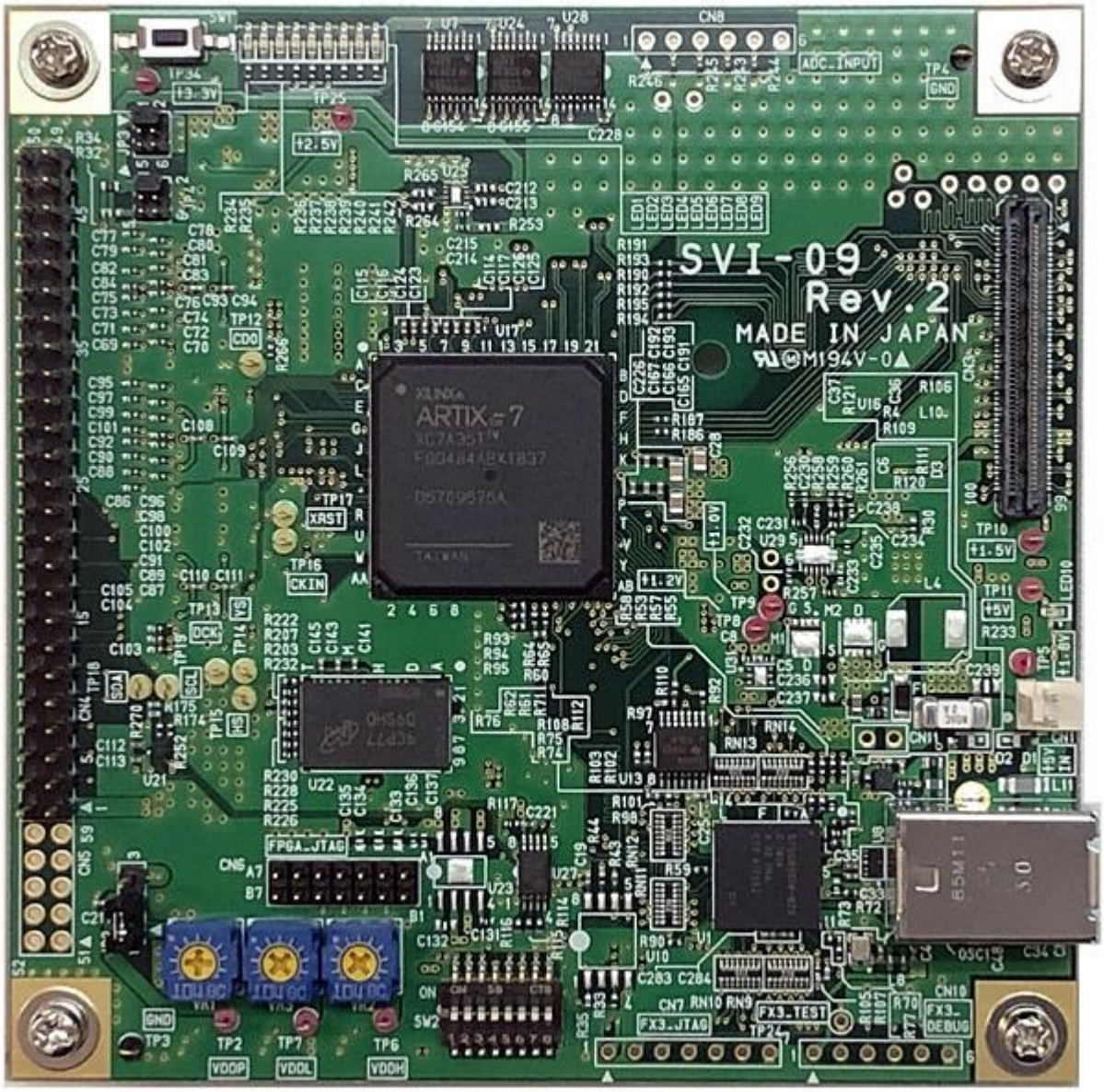
The block diagram of SVI-09 board is shown below.



5. Board Shape

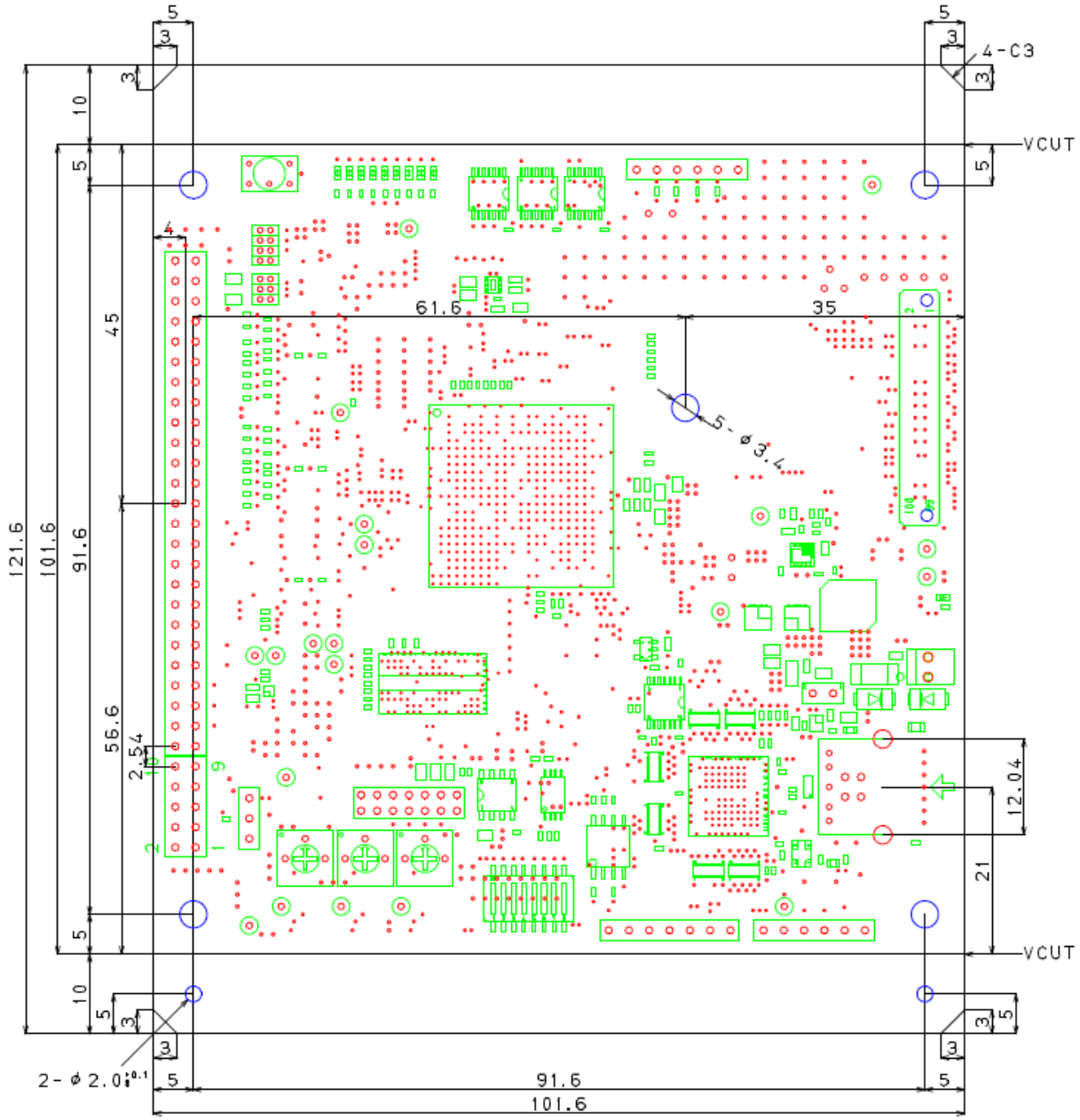
The photo and the drawing of SVI-09 board are shown below.

5.1. Photo



5.2. Drawing

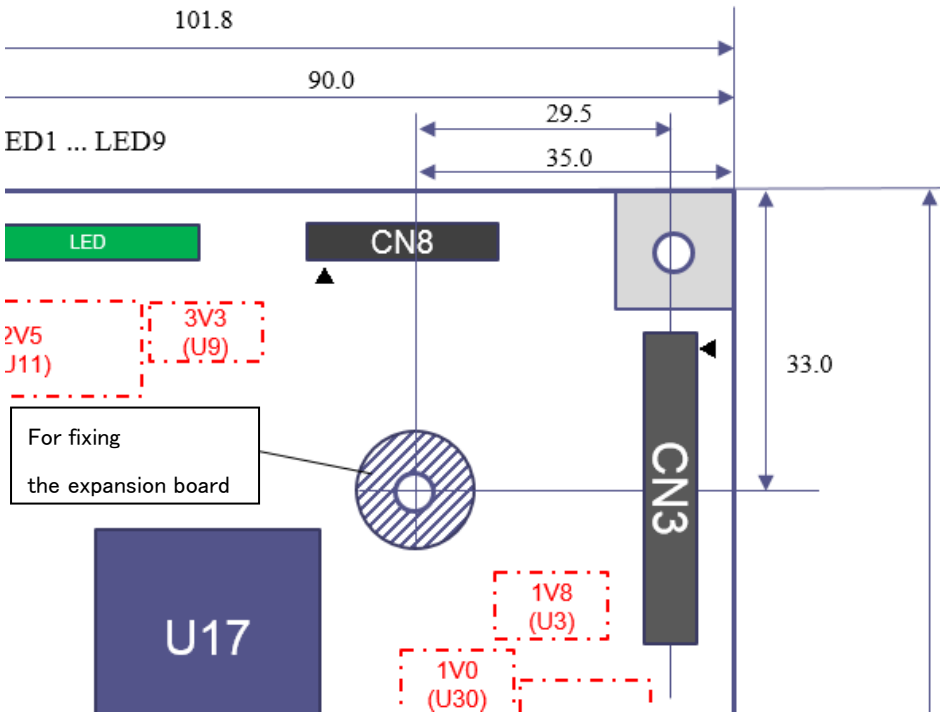
The dimension drawing of SVI-09 board is shown below. The vertical and horizontal dimensions are 101.6 [mm], which is the same as our other current SV series boards, and is smaller than SVI-06/07 (old product) board.



・CN3 Position Relation

The fixing hole positional relationship between CN3 and expansion board is shown below.

The center of CN3 is on the same line as the fixing holes on the expansion board, but not on the line of the four corner holes on the board.



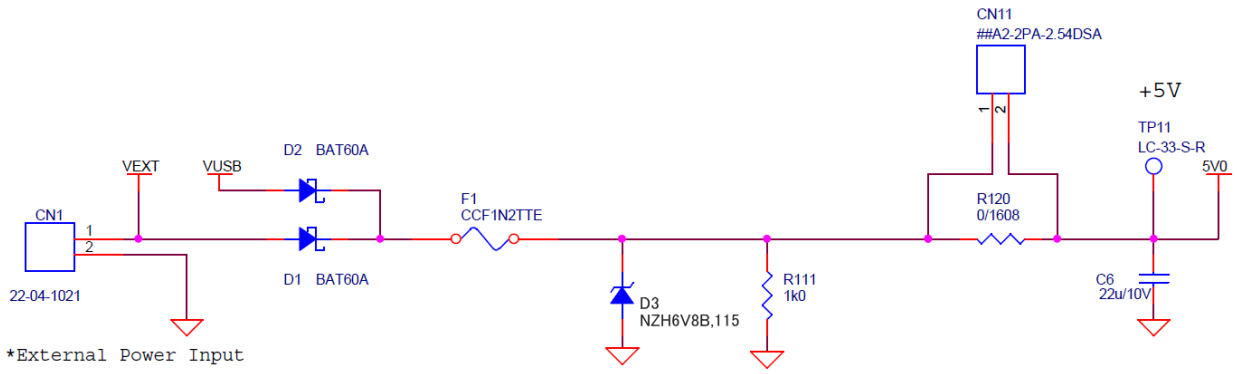
6. Connector Specification

This chapter describes the specifications of connectors that should be considered when connecting to a camera or using normally. Other connectors are described in the Appendix.

6.1. CN1: Sub Power Supply Connector

It is a power connector for use when power is not supplied via USB bus power or when USB bus power can not meet the power capacity.

Connector		22-04-1021: Molex					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	+5V	IN	DC5V Input	2	GND	-	GND



- CN1 and + 5V from the USB connector are connected by diode OR as shown in the above circuit diagram.
- The above figure is the circuit diagram for Rev.2. It is different from Rev.1. Please contact us for Rev.1.

6.2. CN3: Target Connector A

It is a connector for connecting the target image sensor. For signals exceeding the support range of CN 4, 5 such as LVDS signal, you need to use this connector.

- The following pin assignments are only for reference. Detailed functions of pins will be determined according to the system.

Connector		LSHM-150-03.0-F-DV-A-N-K-TR / Samtec	
Pin#	Name	Alternate function (reference)	Description
1	EXCLK1	INCK_1 / INCK	EXCLK [1:0]: Clock Input / Output
2	EXCLK0	INCK_2 / XCLR	
3	EXBUS1	XCLR_1 / VS	EXBUS [17:0]: GPIO
4	EXBUS0	XCLR_2 / HS	
5	EXBUS3	I2CSCL_1 / SPISCK	
6	EXBUS2	I2CSCL_2 / SPIXCE	
7	EXBUS5	I2CSDA_1 / SPISDO	
8	EXBUS4	I2CSDA_2 / SPISDI	
9	GND		
10	GND		
11	EXADC_N1	EXTVS_C	EXADC_N [3:0]: ADC Input - / GPIO
12	EXADC_N0	EXTHS_C	
13	EXADC_P1	PINSWAP_1	EXADC_P [3:0]: ADC Input + / GPIO
14	EXADC_P0	PINSWAP_2	
15	EXADC_N3	GPIO-1_1	
16	EXADC_N2	GPIO-1_2	
17	EXADC_P3	BTA_1	
18	EXADC_P2	BTA_2	
19	GND		
20	GND		

21	EXBUS7	LP-A-N_1	LP-x-N_n: MIPI Low Power (LVCMOS) - (n determines channel number (0-1))
22	EXBUS6	LP-A-N_2	
23	EXBUS9	LP-A-P_1	LP-x-P_n: MIPI Low Power (LVCMOS) +
24	EXBUS8	LP-A-P_2	
25	EXBUS11	LP-B-N_1	
26	EXBUS10	LP-B-N_2	
27	EXBUS13	LP-B-P_1	
28	EXBUS12	LP-B-P_2	
29	EXBUS15	LP-C-N_1	
30	EXBUS14	LP-C-N_2	
31	EXBUS17	LP-C-P_1	
32	EXBUS16	LP-C-P_2	
33	EXLVDS_N1	LP-D-N_1	
34	EXLVDS_N0	LP-D-N_2	
35	EXLVDS_P1	LP-D-P_1	
36	EXLVDS_P0	LP-D-P_2	
37	GND		
38	GND		

Connector		LSHM-150-03.0-F-DV-A-N-K-TR / Samtec	
Pin#	Name	Alternate function (reference)	Description
39	EXLVDS_N3	HS-A-N_1	EXLVDS_N [11:0]: LVDS - (configurable as GPIO) HS-x-N_n: MIPI High Speed (LVDS) -
40	EXLVDS_N2	HS-A-N_2	
41	EXLVDS_P3	HS-A-P_1	EXLVDS_P [11:0]: LVDS + (configurable as GPIO) HS-x-P_n: MIPI High Speed (LVDS) +
42	EXLVDS_P2	HS-A-P_2	
43	GND		
44	GND		
45	EXLVDS_N5	HS-B-N_1	
46	EXLVDS_N4	HS-B-N_2	
47	EXLVDS_P5	HS-B-P_1	
48	EXLVDS_P4	HS-B-P_2	
49	GND		
50	GND		
51	EXLVDS_CLK_N1	HS-E-N_1	EXLVDS_CLK_N [1:0]: LVDS Clock - / GPIO
52	EXLVDS_CLK_N0	HS-E-N_2	
53	EXLVDS_CLK_P1	HS-E-P_1	EXLVDS_CLK_P [1:0]: LVDS Clock - / GPIO
54	EXLVDS_CLK_P0	HS-E-P_2	
55	GND		
56	GND		
57	EXLVDS_N7	HS-C-N_1	
58	EXLVDS_N6	HS-C-N_2	

59	EXLVDS_P7	HS-C-P_1	
60	EXLVDS_P6	HS-C-P_2	
61	GND		
62	GND		
63	EXLVDS_N9	HS-D-N_1	
64	EXLVDS_N8	HS-D-N_2	
65	EXLVDS_P9	HS-D-P_1	
66	EXLVDS_P8	HS-D-P_2	
67	GND		
68	GND		
69	EXLVDS_N11	LP-E-N_1	
70	EXLVDS_N10	LP-E-N_2	
71	EXLVDS_P11	LP-E-P_1	
72	EXLVDS_P10	LP-E-P_2	
73	VDDL		VDDL Power Output
74	VDDH		VDDH Power Output
75	VDDL		
76	VDDH		
77	5V0		Connected to +5V
78	VDDP		VDDP Power Output
79	5V0		
80	VDDP		

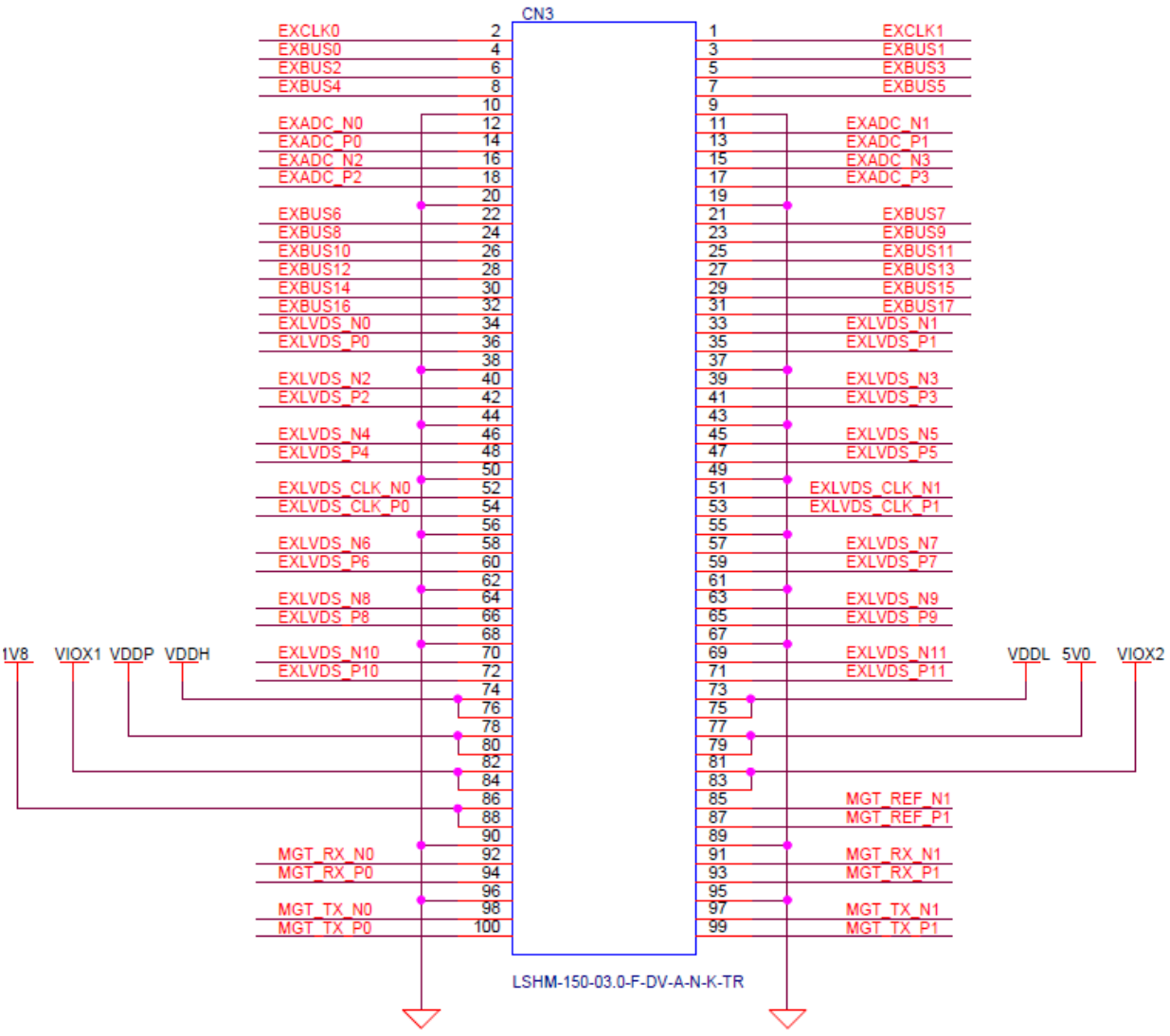
Connector		LSHM-150-03.0-F-DV-A-N-K-TR / Samtec	
Pin#	Name	Alternate function (reference)	Description
81	VIOX2		IO Level Voltage 2
82	VIOX1		IO Level Voltage 1
83	VIOX2		
84	VIOX1		
85	MGT_REF_N1		MGT Referential Input -
86	1V8		Connected to +1.8V
87	MGT_REF_P1		MGT Referential Input +
88	1V8		
89	GND		
90	GND		
91	MGT_RX_N1		MGT Input 1-
92	MGT_RX_N0		MGT Input 0-
93	MGT_RX_P1		MGT Input 1+
94	MGT_RX_P0		MGT Input 0+
95	GND		
96	GND		
97	MGT_TX_N1		MGT Output 1-
98	MGT_TX_N0		MGT Output 0-
99	MGT_TX_P1		MGT Output 1+
100	MGT_TX_P0		MGT Output 0+

- About Single-ended IO Voltage Level

When it is used as a single-ended IO pin, two types of voltage levels can be used with pins. The correspondence is as follows.

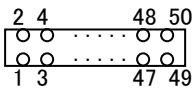
EXCLK[1:0], EXBUS[5:0], EXADC_xx: VDDX1 level

EXBUS[17:6], EXLVDS_xx: VDDX2 level



6.3. CN4: Target Connector B

Top View



It is a connector for connecting the target image sensor.

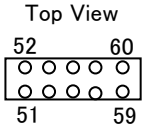
When inputting by parallel connection, input signals from CN 4 (CN 5 is also used if it exceeds 16 bits).

Connector		A1-50PA-2.54DSA: HRS					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	VDDL	OUT	Target IO Power Supply (1.2 – 3.6V adjustable)	2	GND	-	-
3	P0	IN	Input Port 0 / Pixel DATA 16	4	GND	-	-
5	P1	IN	Input Port 1 / DE Input (8-16bit) / Pixel DATA17	6	GND	-	-
7	P2	IN	Input Port 2 / Pixel DATA 18	8	GND	-	-
9	P3	OUT / IN	Output Port 0 / Pixel DATA 24	10	GND	-	-
11	P4	OUT / IN	Output Port 1 / DE Input (24bit) / Pixel DATA 25	12	HSYNC	IN	Horizontal Sync Input
13	VSYN	IN	Vertical Sync Input	14	XRST	OUT	Reset Signal Output
15	VDDH	OUT	Target Power Supply (1.2 – 3.6V adjustable)	16	GND	-	-
17	SDA	IO	I2C_DATA	18	GND	-	-
19	SCL	IO	I2C_CLK	20	GND	-	-
21	DCK	IN	Pixel_CLK (Pixel Clock Input)	22	GND	-	-
23	Y0	IN	Pixel_DATA0	24	GND	-	-
25	Y1	IN	Pixel_DATA1	26	GND	-	-
27	Y2	IN	Pixel_DATA2	28	GND	-	-
29	Y3	IN	Pixel_DATA3	30	GND	-	-
31	Y4	IN	Pixel_DATA4	32	GND	-	-
33	Y5	IN	Pixel_DATA5	34	GND	-	-
35	Y6	IN	Pixel_DATA6	36	GND	-	-
37	Y7	IN	Pixel_DATA7	38	GND	-	-
39	CLKO	OUT	Target drive clock	40	GND	-	-

41	Y8	IN	Pixel_DATA8	42	Y9	IN	Pixel_DATA9
43	Y10	IN	Pixel_DATA10	44	Y11	IN	Pixel_DATA11
45	Y12	IN	Pixel_DATA12	46	Y13	IN	Pixel_DATA13
47	Y14	IN	Pixel_DATA14	48	Y15	IN	Pixel_DATA15
49	VDDP	OUT	Target Power Supply (1.5 – 4.1V adjustable)	50	P5	OUT / IN	Output Port 2 / Pixel DATA 26

6.4. CN5: Target Connector C

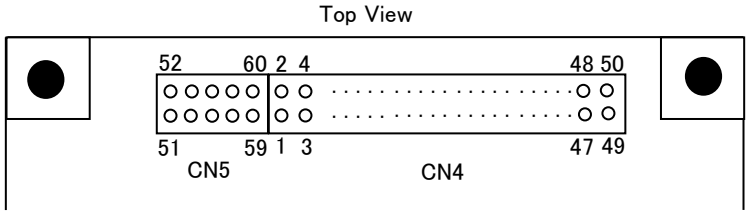
It is a connector for connecting the target image sensor.



Connector	A1-10PA-2.54DSA: HRS						
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
51	P6	OUT / IN	Output Port 3 / Pixel DATA 27	52	P7	OUT / IN	Output Port 4 / Pixel DATA 28
53	P8	OUT / IN	Output Port 5/ Pixel DATA 29	54	P9	OUT / IN	Output Port 6/ Pixel DATA 30
55	P10	OUT / IN	Output Port 7/ Pixel DATA 31	56	P11	IN	Input Port 3/ Pixel DATA 19
57	P12	IN	Input Port 4/ Pixel DATA 20	58	P13	IN	Input Port 5/ Pixel DATA 21
59	P14	IN	Input Port 6/ Pixel DATA 22	60	P15	IN	Input Port 7/ Pixel DATA 23

- CN5 is optional; this connector is not mounted as standard SVI-09.
- The input / output direction of Pixel_DATA [31: 24] is changed according to the input bit width setting.

6.5. Position Relationship between CN4 and CN5



- These connectors, together with CN4 and CN5, can be used as a 60P pin header.
- The 60-pin connector is "HRS: HIF3BA-60D-2.54R"when connected by cable, and is "HRS: HIF3H-60DA-2.54DSA(71)" when connected by board-to-board connect.

6.6. Input Data Format

When YUV or RGB24 format image sensor is connected to SVI-09 board, Connect wires according to the table below.

Format	YUV4:2:2			RGB24
Bit Width	8bit (UYVY/YUY2)	16bit (UYVY)	32bit (UYVY)	24bit
Pixel_DATA [31:24]	-	-	V	-
Pixel_DATA [23:16]	-	-	Y	R
Pixel_DATA [15:8]	-	U, V	U	B
Pixel_DATA [7:0]	Y, U, V	Y	Y	G

- VS, HS, DCK polarity is arbitrary.

7. Details of Each Part

7.1. SW1: Push Switch

Normally it is not used.

7.2. SW2: DIP Switch

This is an 8-bit switch for setting various operations in each mode of SVI-09. The setting by switch SW2 is as follows.

7.2.1. Vendor mode

Number #	Name	OFF	ON
1 2	I2C transfer rate	1 OFF 2 OFF 400Kbps *default 1 ON 2 OFF 100Kbps 1 OFF 2 ON 200Kbps 1 ON 2 ON 100Kbps	
3 4	Board number	3 OFF 4 OFF 0 *default 3 ON 4 OFF 1 3 OFF 4 ON 2 3 ON 4 ON 3	
5	Master clock division	1/1	1/2 *default
6	Camera power setting	Power on at startup *default	Power off at startup
7 8	Operation mode setting (at startup)	7 OFF 8 OFF UVC mode 7 ON 8 OFF Update mode 7 ON 8 ON Forbidden 7 OFF 8 ON Vendor mode *default	

7.2.2. UVC mode

Number #	Name	OFF	ON
1	Camera input data width setting 1	8bit x 2 CLK	16bit x 1 CLK (YUV) 24bit x 1 CLK (RGB)
2	Test pattern output (UVC mode only)	Normal operation	Test pattern output
3	Camera input data width setting 2	(Follows DIP SW 1)	32bit x 1/2 CLK
4	-	-	-
5	-	-	-
6	-	-	-
7	Operation mode setting (at startup)	7 OFF 8 OFF UVC mode * default 7 ON 8 OFF Update mode 7 ON 8 ON Forbidden 7 OFF 8 ON Vender mode	
8			

In UVC mode, you set the signal polarity or resolution with control software "SVMctl.exe".

* If you use the LAN I/F board, the settings of 7 and 8 are different. Refer to the LAN I/F board hardware specification for settings.

7.3. LED1-10: LED Indicator

LED on this board display the operating status of the board or FPGA.

LED#	Description
1	When lit, it indicates that power is being supplied to the target. This is a red LED.
2	When lit, it indicates that the clock supplied to the target is locked.
3	When lit, it indicates that a synchronized signal related to the video input from the target is being detected.
4	It blinks at one-third of the cycle of VSYNC sync signal from the target. When the input video is 30fps, it blinks 5 times per second.
5	When lit, it indicates that video frame writing to frame memory is idle.
6	When lit, it indicates that the frame information management table in the secondary side is used when the video frame is first written to frame memory. The default is on the primary side, and the light is off.
7	When the light is on, it indicates that the video frame can be written to the frame memory.
8	When lit, it indicates that the video frame is being read and transmitted from the frame memory.

9	<Vendor mode> When lit, it indicates that USB output reading and DMA transfer is complete. <UVC mode> It blinks at one-third of the cycle of the FV (Frame Valid) pulse on the UVC output.
10	When lit, it indicates that power is being supplied to the board. This is a red LED.

7.4. **RV1, RV2, RV3**: VDDH, VDDL, VDDP Adjustment Variable Resistor

These are variable resistors for the target device to regulate the power supply generated by the SVI-09 board. VDDL, VDDH can be adjusted from 1.2V～3.6V. VDDP can be adjusted from 1.5V - 4.1V.

Since VDDL is connected to voltage translator ICs, this voltage level must be equal to the parallel input signal level and GPIO voltage level. On the other hand, VDDH and VDDP are just connected to the target connector and are not used inside the board. Both voltages can be used as the power supply of external target device. For detail of VDDL, VDDH and VDDP, please refer to section 9.

In default, VDDL, VDDH, and VDDP are set to 3.3 V. You must adjust them according to the voltage of the target before use.

7.5. **JP2:** Jumper for VDDP Selection

The VDDP power supply output of SVI-09 is selected by JP2 from two systems ; +5V output from USB power supply and variable power supply from on-board regulator.

JP2	VDDP
1-2 short circuit	variable power supply
2-3 short circuit	VUSB (+5V)

7.6. **JP3, JP4:** Jumpers for Setting VIOX1, VIOX2

On the SVI-09 board, the connector CN3 is newly mouneted in addition to the IO connector mounted on the conventional board. For single-ended IO of CN3, two IO voltages (VIOX1, VIOX2) can be set, and these IO voltages are set by JP3, JP4. The voltage setting values are shown in the table below. **Do not turn on SVI-09 without inserting the JP3 and JP4 jumper pins, as this may lead to breakdown.**

For the correspondence between VIOX1, VIOX2 and each IO pin of CN3, refer to the pin assignment chart.

JP3 voltage setting (VIOX1)

JP3	VIOX1
1-2 short circuit	1.8V
3-4 short circuit	2.5V
5-6 short circuit	3.3V

JP4 voltage setting (VIOX2)

JP4	VIOX2
1-2 short circuit	1.8V
3-4 short circuit	2.5V
5-6 short circuit	3.3V

8. Check Terminal

TP6: VDDH check terminal (red)

This is the check terminal used to adjust the VDDH.

TP7: VDDL check terminal (red)

This is the check terminal used to adjust the VDDL.

TP5, 8, 9, 10, 11, 25. 34: Voltage check terminal (red)

These are the check terminals for each supply voltage required by SVI-09 operation.

TP3, 4: GND check terminal (black)

These are the GND terminals used for voltage adjustment.

*The above are descriptions for Rev.2. These are different from Rev.1. Please contact us for Rev.1.

9. Target Power Supply

In addition to the power supply of the IC mounted into the board, SVI-09 has variable voltage power supplies of multiple systems for the target device.

9.1. **VDDH**: System Power Supply for Target Device

VDDH is designed to be used as the power supply voltage for image sensors and target devices. It can be adjusted by the variable resistor RV1 mounted on the board, adjusted about from1.2V to 3.6V, and can output about 200mA of current. The default setting is +3.3V.

9.2. **VDDL**: IO Power Supply for Target Device

VDDL is designed to be used as IO power supply for image sensors and target devices. It can be adjusted by the variable resistor RV2 mounted on the board, adjusted about from1.2V to 3.6V, and can output about 200mA of current.

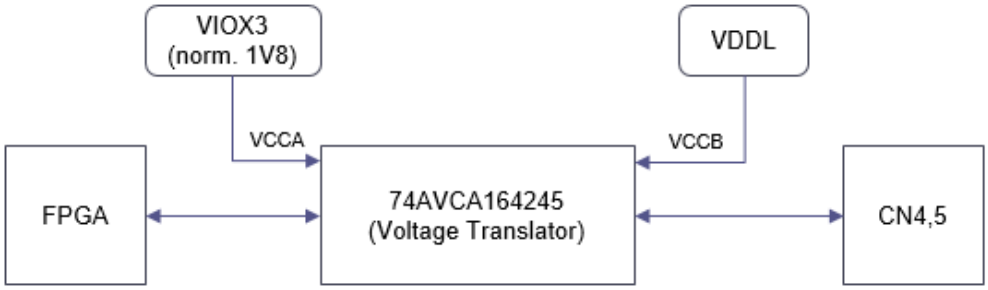
The SVI-09 is equipped with a level converter IC, and **when you use CN 4 and 5**, IO signals are converted from VDDL level to internal IO level. Thus, **even if VDDL is not used in the target device, VDDL must be adjusted to the output IO voltage level of the target.**

When you use CN3, the IO voltage (VIOX1, VIOX2) of CN3 is set independently from VDDL because it is selected by jumper JP3 and 4. The default setting is +3.3V.

9.3. **VDDP**: Auxiliary Power Supply for Target Device

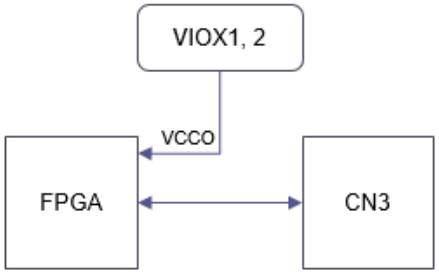
VDDP is designed to be used as auxiliary power supply for image sensors and target devices. When the status of the jumper JP2 is short-circuited between 1 and 2, VDDP can be adjusted with the variable resistor RV3 mounted on the board, adjusted about from 1.5V to 4.1V, and can output about 200 mA of current. When JP2 is short-circuited between 2 and 3, USB power supply +5V is output directly to VDDP. The default setting is +3.3V.

9.4. CN4 and 5 IO Schematic Diagram



- The IO voltage of each pin depends on the voltage of VDDL.

9.5. CN3 IO Schematic Diagram



- The IO voltage of each pin depends on the voltage of VIOX1, VIOX2.

10. Notes

For proper use of the board, be sure to observe the following precautions.

1. To update the farm and FPGA, use dedicated control software from the host PC.
2. When connecting and disconnecting targets, be sure to turn off the power supply of SVI-09.
3. Use a power supply that has a sufficient current capacity to supply power to the board, and supply power from a PC at your own risk. We are not responsible for any damage to your PC by any chance.
4. The contents of this document may be changed in the future without notice.
5. Reprinting of part or the whole of the contents of this document is strictly forbidden.
6. If you notice anything incorrect, omissions or errors, please contact NetVision.
   sv-support@net-vision.co.jp

11. Appendix

11.1. CN2: USB3.0 Connector

CN2 is USB 3.0 connector for connecting to the host PC. You can use a commercially available USB 3.0 cable. This connector is also used to supply power to SVI-09.

Connector		USB30B-09K-PC: JC Electronics Corporation					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	VBUS	IN	+ 5v Bus Power	2	D-	I/O	USB 2.0 Differential Pair-
3	D+	I/O	USB 2.0 Differential Pair+	4	GND	-	GND for Power
5	SSRX-	IN	USB 3.0 Reception Differential pair -	6	SSRX+	IN	USB 3.0 Reception Differential pair +
7	GND DRAIN	-	GND for Signal	8	SSTX-	OUT	USB 3.0 Transmission Differential pair -
9	SSTX+	OUT	USB 3.0 Transmission Differential pair +				

11.2. CN6: FPGA-JTAG Connector

CN6 is the JTAG port used to write to the SPI-ROM of the FPGA bit stream or to debug a running FPGA. You do not need to use it in normal operation.

*The direction is seen from the FPGA.

Connector		A3B-14PA-2DSA(71): HRS					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	GND	-		2	VREF	OUT	Reference Voltage (3.3V)
3	GND	-		4	TMS	IN	JTAG-TMS
5	GND	-		6	TCK	IN	JTAG-TCK
7	GND	-		8	TDO	OUT	JTAG-TDO
9	GND	-		10	TDI	IN	JTAG-TDI
11	GND	-		12	NC	-	Disconnected
13	GND	-		14	NC	-	Disconnected

***We do not guarantee the operation when you use it.**

11.3. CN7: FX3-JTAG Connector

CN7 is the JTAG port used to debug the FX3 firmware. You do not need to use it in normal operation.

*The direction is seen from the FPGA.

Connector		A2-7PA-2.54DSA(71): HRS					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	+3.3V	OUT	Reference Voltage (3.3V)	2	TMS	IN	JTAG-TMS
3	TCK	IN	JTAG-TCK	4	TDO	OUT	JTAG-TDO
5	TDI	IN	JTAG-TDI	6	TRST	OUT	Reset
7	GND	-					

*CN7 is optional. The PIN header is not mounted.
***We do not guarantee the operation when you use it.**