Image generator

[SVO-03]

Hardware Specification

Rev.1.1

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	2018/07/02	New File (Equivalent to Japanese version 1.2)	S.Usuba
1.1	2019/10/24	Revised translation (Equivalent to Japanese version 1.7)	F.Tanabe

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1. Outline

This document is a hardware specification of "SVO-03", an I/F board that outputs video footage of images stored on a PC as if it were a camera or an image sensor.

SVO-03 has three modes: "USB input mode", "HDMI input and parallel output mode", and "HDMI input and USB output mode". These modes can be switched using the DIP switches (SW2) #7 and #8 on the board.

In USB input mode, you can connect to a PC with a USB3.0 interface and easily output images to the target board in real time.

HDMI input and parallel output modes support commonly used parallel video signal formats. Using this mode, you can smoothly develop video processing devices with parallel signal inputs.

The HDMI input and USB output modes support USB Video Class (UVC), which is a USB standard, so you can import video to a PC without a driver, regardless of OS or software. In addition, it supports uncompressed video up to 1920x1080 60FPS by USB3.0 high-speed transfer.

1.1. Functions of SVO-03

- Convert parallel signals from video files on a computer
- Convert HDMI signal to parallel signal
- Convert HDMI signal to USB3.0 (UVC)

1.2. Specifications (USB input mode)

- Power supply: USB bus power supply (external power supply is possible) / + 5V 0.65A typ.
- Input: USB3.0 connector
- Output resolution: Max 4093 x 4093 pixel
- Output frame rate: Any
- Output pixel format: YUV422 / RGB24 / Raw8,10,12 / RGB565
- Output bit width: YUV (8bit, 16bit, 32bit) / RGB24 (24bit)
- Output voltage level: Single-ended 1.8 – 3.6V CMOS (adjustable)
- Output connector: Our SV series standard (50 / 60pin, 2.54mm pin header)
- Input resolution, frame rate, pixel format: same as output [1]

[1] When the input format is AVI format, the pixel format on the file supports YUV or RGB24 (DIB). In the case of FRM format, Raw and RGB565 are supported in addition to the above pixel formats.

1.3. Specifications (HDMI input and parallel output modes)

- Power supply: USB bus power supply (external power supply is possible) / + 5V 0.65A typ.
- Input: HDMI1.4 (RGB4: 4: 4)
- Output resolution: 1280x720 / 1920x1080 pixel [2]
- Output frame rate: 30/60 FPS (* pixel clock within 150MHz)
- Output pixel format: YUV (UYVY, YUY2), RGB24 (RGB8: 8: 8) uncompressed
- Output bit width: YUV (8bit, 16bit, 32bit) / RGB24 (24bit)
- Output voltage level: Single-ended 1.8 – 3.6V CMOS (adjustable)
- Output connector: Our SV series standard (50 / 60pin, 2.54mm pin header)
- Input resolution, frame rate, pixel format: same as output

[2] It is possible to output with different resolution by setting EDID and signal timing from our application "SVOCtl".

1.4. Specifications (HDMI input and USB output mode)

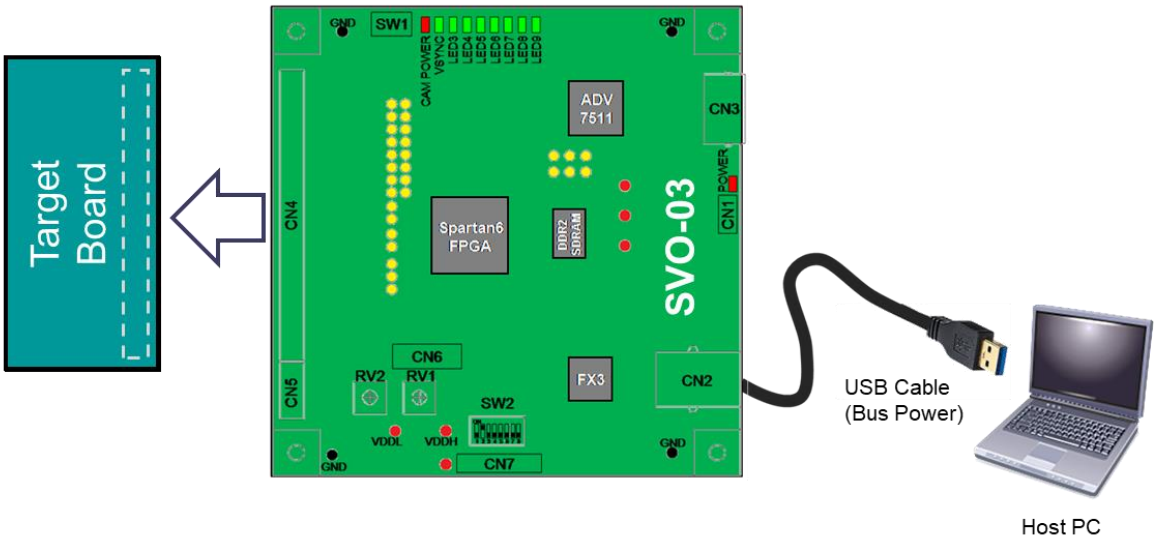
- Power supply: USB bus power supply (external power supply is possible) / + 5V 0.65A typ.
- Input: HDMI1.4 (RGB4: 4: 4)
- Output resolution: 1280x720 / 1920x1080 pixel
- Output frame rate: same as input
- Output pixel format: YUV (UYVY, YUY2), RGB24 (RGB8: 8: 8) uncompressed
- Output: USB Video Class (UVC) compliant
- Input resolution, pixel format: same as output

2. Operation details of USB input mode

2.1. Features of USB input mode

- Converts uncompressed .avi or .frm files saved on the PC to parallel signals and outputs them.
- Since transfer is performed without compression, image quality is not impaired and it is ideal for evaluation tests and algorithm development.
- Compatible with Windows OS.
- Dedicated video output software (SVOGenerator) is included in the supplied CD.
- Equipped with a USB3.0 device controller, so images and video files saved on the host PC can be transferred at high speed via USB3.0 (5Gbps), and video signals can be output in digital parallel. It has a function as a generator (hereinafter referred to as USB version).
- Select multiple boards from the application via USB connection to the host PC, pixel clock frequency for video output, timing and polarity of synchronization signals such as VS / HS, and details such as Embedded Sync. (SAV / EAV) Settings and controls.
- Since DDR2-SDRAM (128MByte) is installed as a frame memory, it can support various output timings according to the target, and image output without data omission and line omission is possible. (It may not be guaranteed depending on the operation mode and transfer settings.)
- External clock input (synchronization with the pixel clock of the external output device), external synchronization input (video synchronization signal of the external output device as the master and video synchronization with this device as the slave), external trigger input (external output device) Because it supports start / stop control by the trigger of, it can be synchronized between multiple SVO-03 boards or with other devices.
- The target connection side is 60 pins with 2 rows of 2.54mm pitch and is completely pin compatible with the existing SVO-02 and other SV series, so it can be connected immediately to the target such as your camera evaluation board. I can do it.
- The output hardware specifications for target connection are 16-bit CMOS parallel data, VSYNC, HSYNC, and pixel clock are output as synchronization signals, and the pixel clock output is up to 150MHz.
- Equipped with 8bit general-purpose output port / 8bit general-purpose input port (switchable to each other in units of 8bit), so setting to the target evaluation board, status reading, etc. are possible.
- By combining the above general-purpose ports as 16-bit output, 32-bit data output is also possible. (Currently, data output with a bit width larger than 16 bits is an option.)
- Supports DDR output, and data and sync signals can be output at twice the bit rate with respect to the pixel clock, so image output that requires high transfer rates such as 1080p / 60fps is standard. Can be output on a 16-bit data bus.
- Pixel clock output supports any frequency by using the built-in PLL and DCM in the built-in FPGA.
- The output image format is 8bit x 2CLKs or 16bit x 1CLK and supports YUV4: 2: 2 format. (It is an option, but it is possible to increase the lineup.)
- The power supply of the SVO-03 board operates by supplying 5V power from the USB connector. Since power is supplied from the USB port of the PC via the USB cable, a dedicated AC adapter is usually not required.
- The DIP switch No. 7 is set to OFF and No. 8 is set to ON to start up as USB input mode.

2.2. Connection structure of USB input mode



2.3. About power input

Since the SVO-03 board does not require a dedicated power adapter, it can be powered by USB connection to the host PC. In the image output operation state when the target is not connected, the USB version consumes about **620mA** for USB bus power (5V) input. In the image output with the target connected, the amount of current will increase further, so use a USB cable with sufficient current capacity for power supply and connect it to the USB3.0 port of the host PC.

2.4. About power supply from USB port of PC etc.

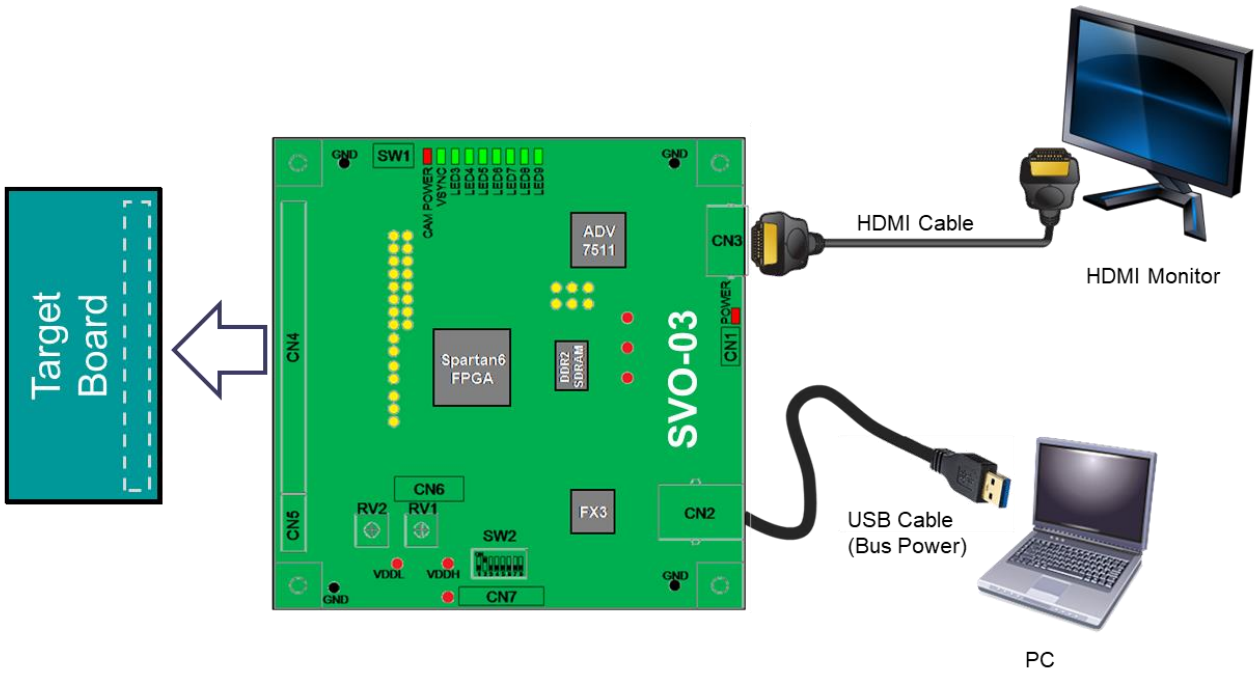
It is possible to operate with USB power supply from a PC, etc., but it is determined on the USB specification as a **maximum of 500mA** for USB2.0 port and a **maximum of 900mA** for USB3.0 port. In addition, connection with a battery-powered mobile PC may limit power, so connection with a PC connected to an AC power supply is recommended.

3. Operation details of HDMI input and parallel output mode

3.1. Features of HDMI input and parallel output modes

- The video signal from the HDMI connector is converted into a parallel signal and output.
- Since transfer is performed without compression, image quality is not impaired and it is ideal for evaluation tests and algorithm development.
- Utility software for setting EDID and signal timing is included.
- Even when the above software is not used, resolutions of 1920x1080 and 1280x720 are supported as standard by setting the DIP switch.
- The target connection side is 60 pins with 2 rows of 2.54mm pitch and is completely pin compatible with the existing SVO-02 and other SV series, so it can be connected immediately to the target such as your camera evaluation board. I can do it.
- It starts as HDMI input and parallel output mode by setting DIP switch No. 8 to OFF and starting.

3.2. Connection structure of HDMI input and parallel output mode

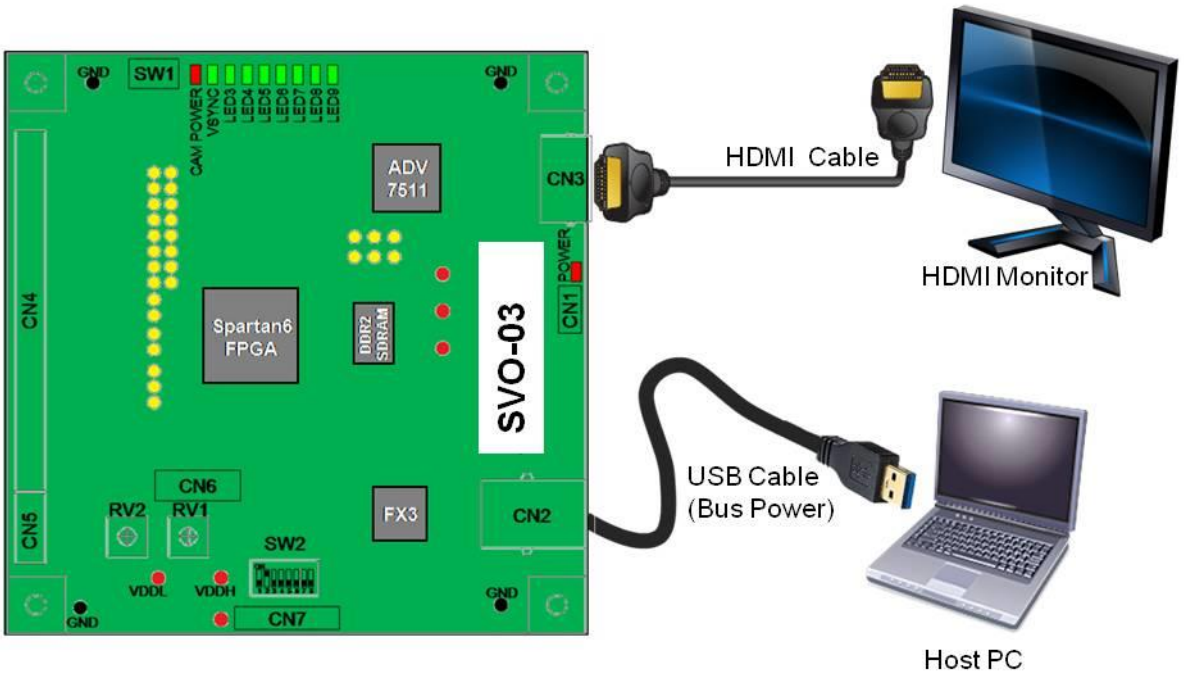


4. Operation details of HDMI input and USB output modes

4.1. Features of HDMI input and USB output modes

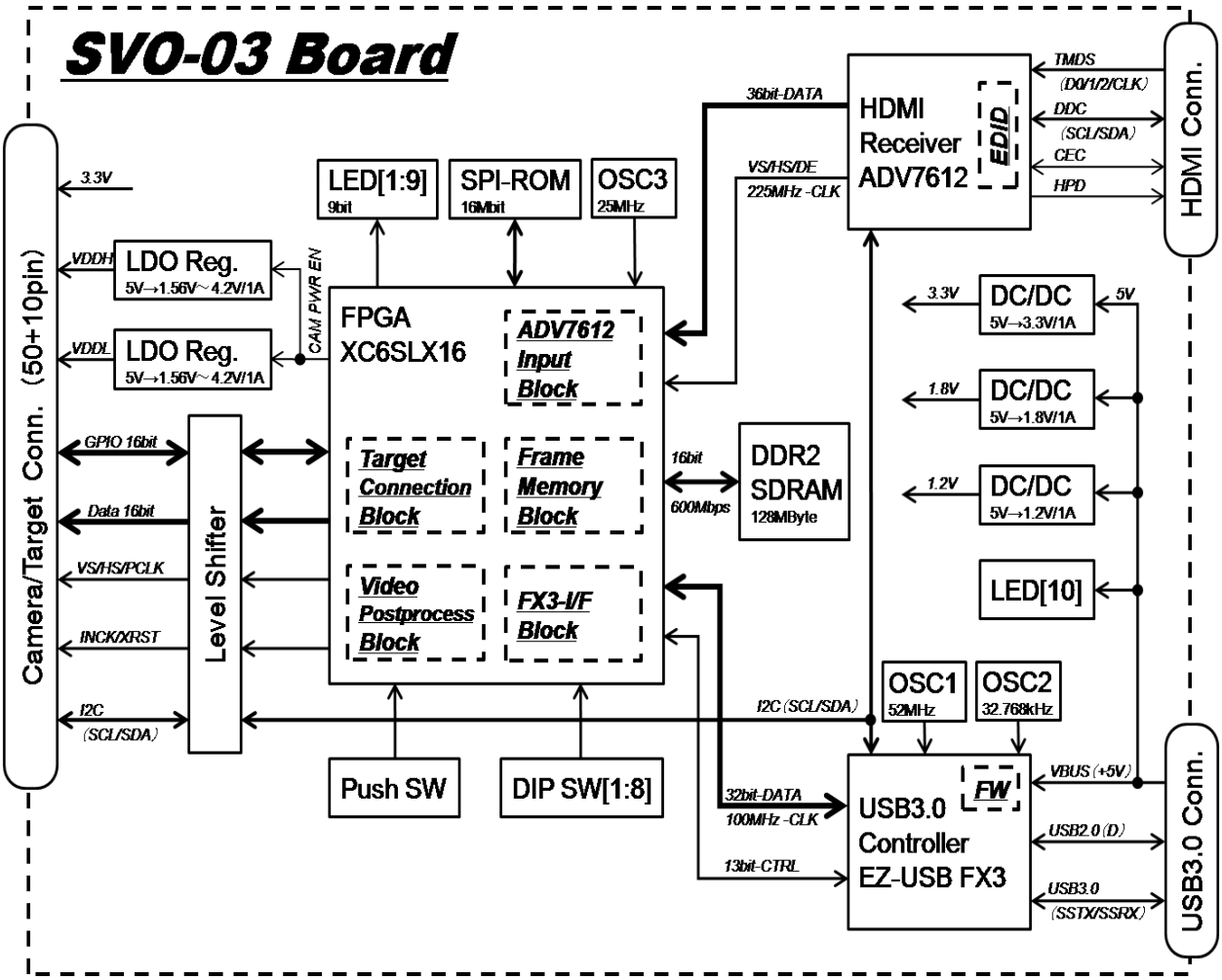
- The video signal from the HDMI connector is output to the PC via USB connection.
- Since transfer is performed without compression, image quality is not impaired and it is ideal for evaluation tests and algorithm development.
- Dedicated DirectShow capture software (NVCap) is included in the included CD.
- Up to 3.2Gbps (theoretical value) video data can be imported without compression by high-speed USB3.0 transfer.
- Set the pixel format, resolution, and frame rate with the DIP switch.
- Setting from the PC is basically unnecessary.
- The USB3.0 chip is equipped with Cypress EZ-USB FX3.
- By starting with DIP switch No. 7 set to ON and No. 8 set to ON, it starts as HDMI input and USB output mode.

4.2. Connection structure of HDMI input and USB output modes



5. SVO-03 block diagram

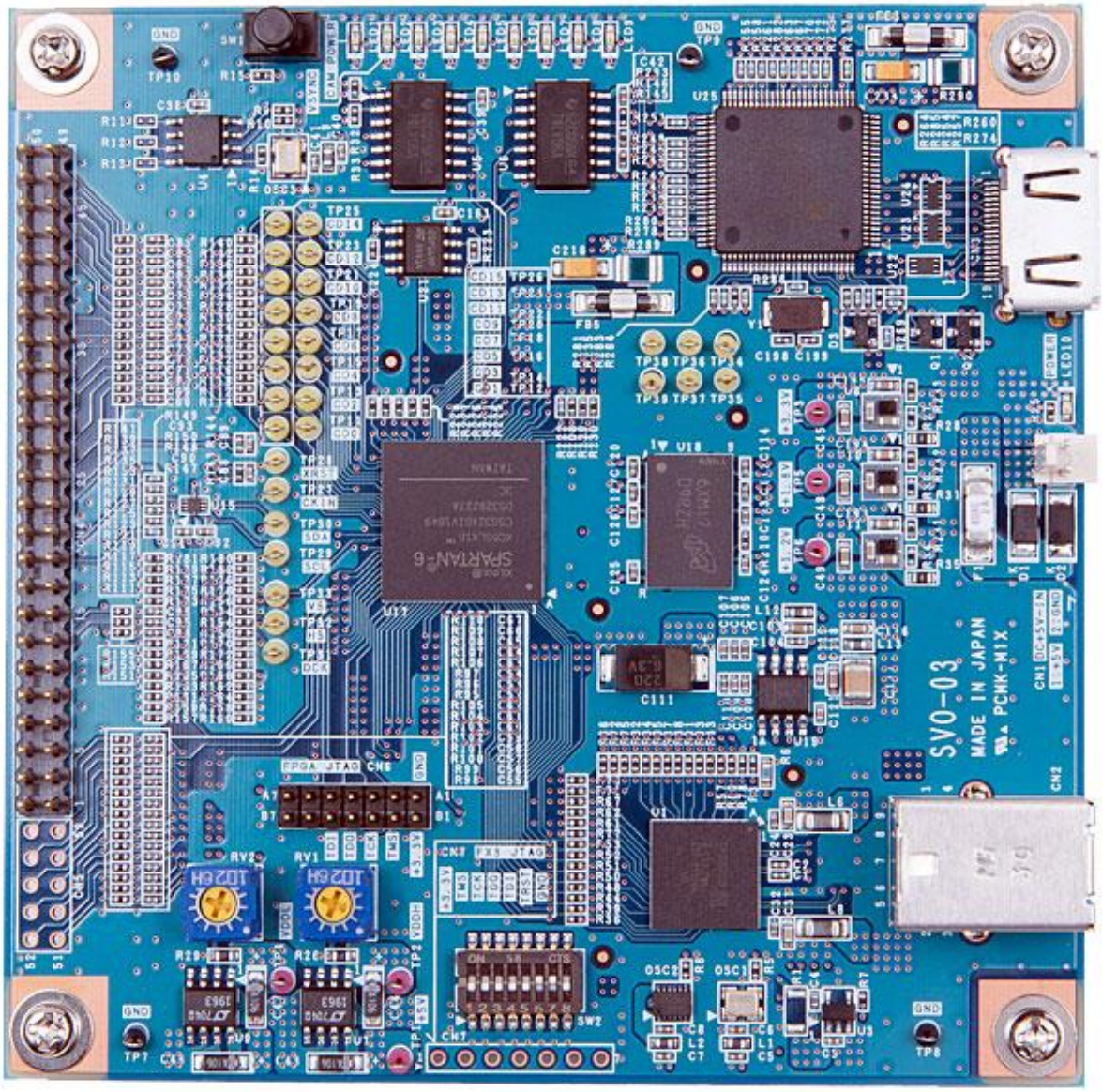
A schematic block diagram of SVO-03 is shown below.



6. SVO-03 board shape

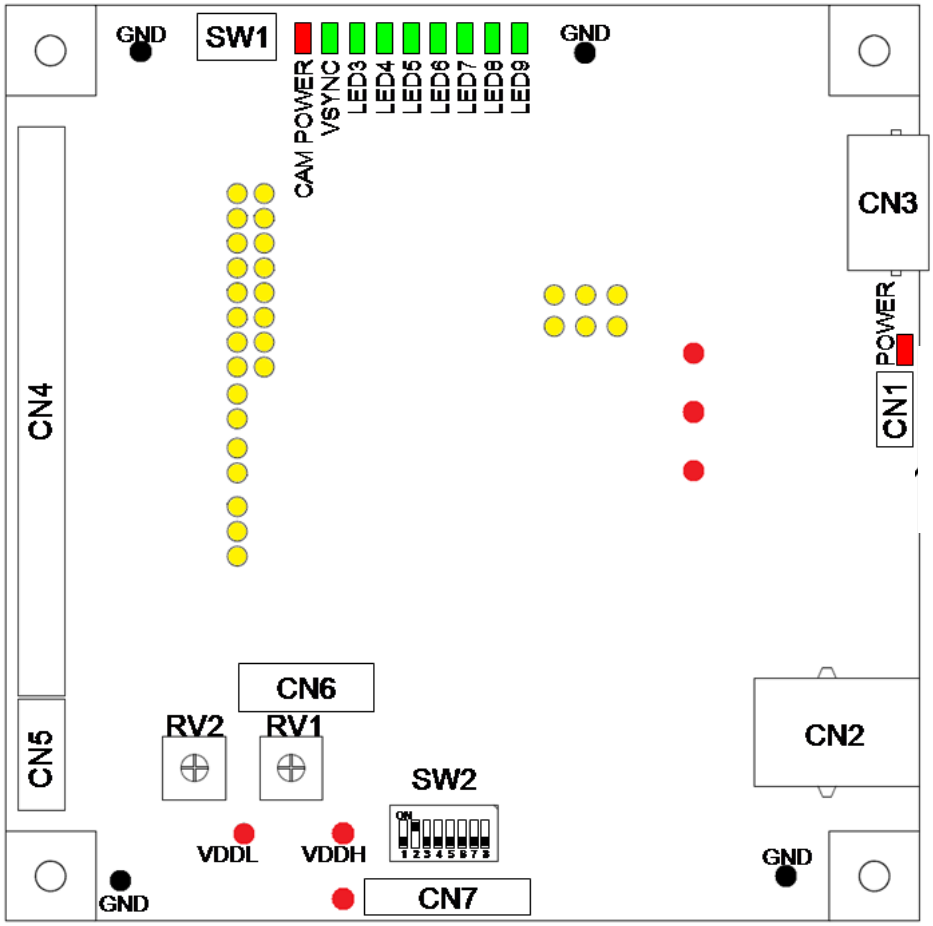
Here is a photo and a picture of the outline of the SVO-03 board.

6.1. SVO-03 appearance photo



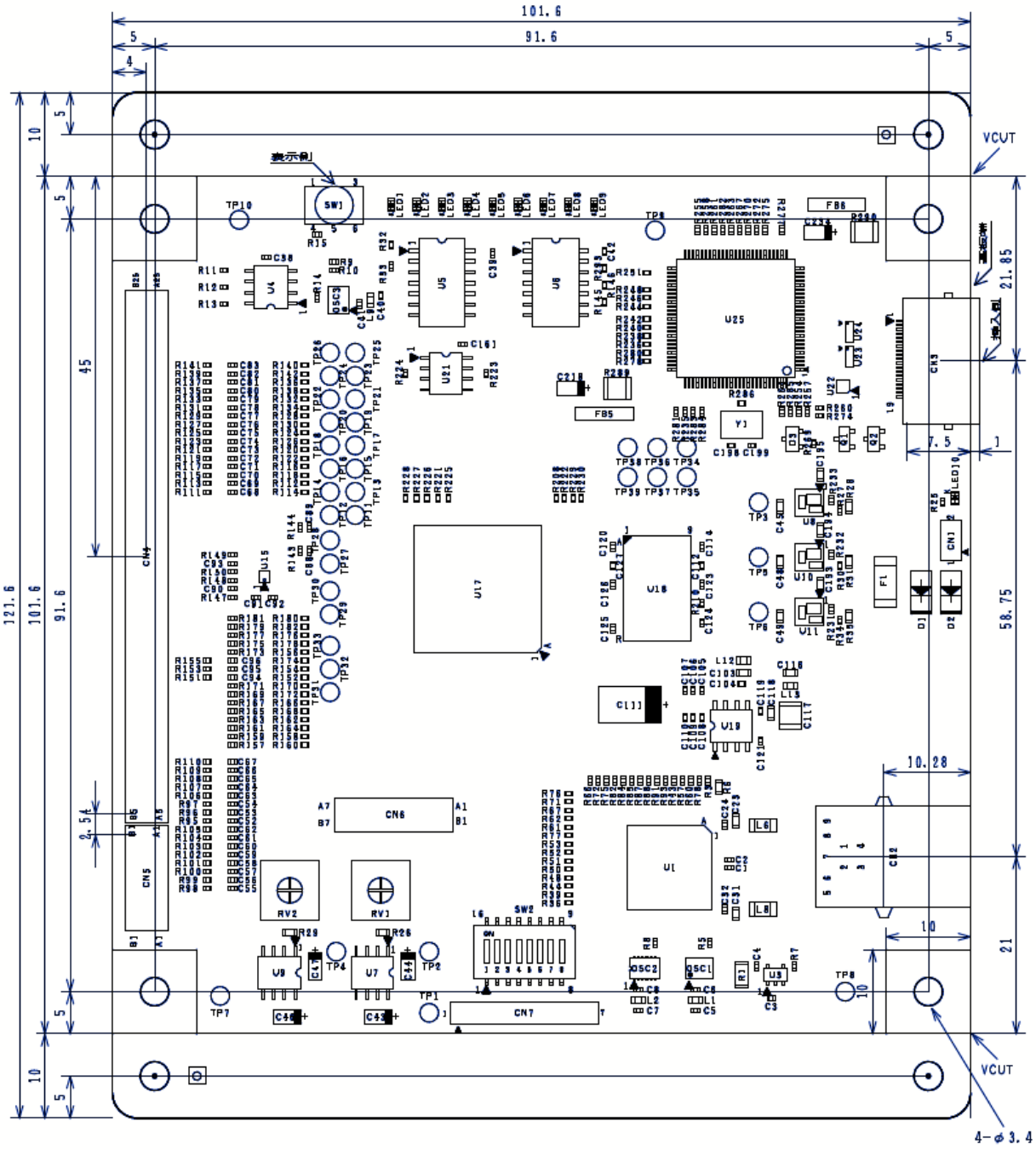
6.2. SVO-03 board layout

Below is a schematic layout of the SVO-03 board. Only parts that can be operated or checked by the user, such as connectors, switches, and light emitting diodes on the board, are shown.



6.3. SVO-03 board dimensions

The following is a dimensional drawing of the SVO-03 board. The actual board does not include the 10mm part up to the VCUT at the top and bottom, respectively, and the vertical size is 101.6 [mm] like other SV series.



7. SVO-03 Connector specifications

7.1. **CN1:** External Power Input Connector

This power connector is used when the USB bus power cannot satisfy the power capacity or when power is not supplied via USB bus power.

Connector		5045-02A(22-11-1021): Molex					
Pin	Name	DIR	Description	Pin	Name	DIR	Description
1	+5V	IN	DC5V Input	2	GND	-	GND

+5V (DC5V_IN) from CN1 and + 5V (USB_VBUS) from the USB connector are connected by a diode OR as shown in the above circuit diagram, and are used as the board internal power supply (+ 5V).

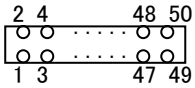
The direction of pins 1 and 2 of CN1 is silk-printed at the position on the USB connector side on the board.

7.2. **CN4:** Target Connector

CN4 is a connector for connecting targets.

※The direction is the direction seen from SVO-03.

Top View



Connector		A1-50PA-2.54DSA: HRS					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	VDD_L※	OUT	Target IO Power Supply (1.56～4.20V adjustable)	2	GND	-	-
3	P0	OUT	Output Port 0 Internal VS output for Fsync Master	4	GND	-	-
5	P1	OUT	Output Port 1 DE Output	6	GND	-	-
7	P2	OUT	Output Port 2	8	GND	-	-
9	P3	IN	Input Port 0 PIXEL_CLK input for external synchronization	10	GND	-	-
11	P4	IN	Input Port 1 VS Input for external synchronization	12	HS	OUT	Horizontal Sync Input
13	VS	OUT	Vertical Sync Input	14	XRST※	OUT	Reset Output
15	VDD_H※	OUT	Target Power Supply (1.6 - 4.2V adjustable)	16	GND	-	-
17	SDA	I/O	I2C_DATA	18	GND	-	-

19	SCL	I/O	I2C_CLK	20	GND	–	–
21	DCK	OUT	Pixel_CLK	22	GND	–	–
23	Y0	OUT	Pixel_DATA0	24	GND	–	–
25	Y1	OUT	Pixel_DATA1	26	GND	–	–
27	Y2	OUT	Pixel_DATA2	28	GND	–	–
29	Y3	OUT	Pixel_DATA3	30	GND	–	–
31	Y4	OUT	Pixel_DATA4	32	GND	–	–
33	Y5	OUT	Pixel_DATA5	34	GND	–	–
35	Y6	OUT	Pixel_DATA6	36	GND	–	–
37	Y7	OUT	Pixel_DATA7	38	GND	–	–
39	DE※	OUT	DE Output	40	GND	–	–
41	Y8	OUT	Pixel_DATA8	42	Y9	OUT	Pixel_DATA9
43	Y10	OUT	Pixel_DATA10	44	Y11	OUT	Pixel_DATA11
45	Y12	OUT	Pixel_DATA12	46	Y13	OUT	Pixel_DATA13
47	Y14	OUT	Pixel_DATA14	48	Y15	OUT	Pixel_DATA15
49	+3.3V※	OUT	+3.3V Output (up to 0.3A)	50	P5	IN	Input Port 2 HS input for external synchronization

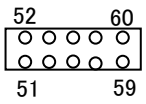
※The signal is not able to change direction, and it always becomes the output state. When connecting to a SVI board, you must cut the target line.

7.3. **CN5**: Target Connector (Optional)

CN4 is a connector for connecting targets.

※The direction is the direction seen from SVO-03.

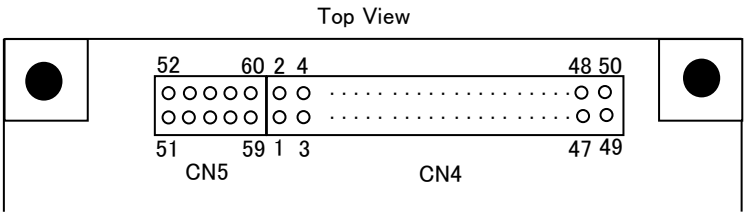
Top View



Connector		A1-10PA-2.54DSA: HRS					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
51	P6	IN	Input Port 3	52	P7	IN	Input Port 4
53	P8	IN	Input Port 5	54	P9	IN	Input Port 6
55	P10	IN	Input Port 7	56	P11	OUT	Output Port 3
57	P12	OUT	Output Port 4	58	P13	OUT	Output Port 5
59	P14	OUT	Output Port 6	60	P15	OUT	Output Port 7

- CN5 about that is optional. The PIN header is not implemented.
- For 24bit image output and 32bit image output, CN5 must be implemented.
- See also: "13 8bit/16bit/24bit/32bit image output CN4, Cn5 pin assignment".

7.4. Relationships between **CN4 and CN5**



- Together with CN5 and CN4, these connectors can be used as a 60P pin header.
- The 60-pin connection connector becomes "Hirose Electric: HIF3BA-60D-2.54R"when connected by cable.
- The 60-pin connection connector becomes "Hirose Electric: HIF3H-60DA-2.54DSA(71)" when connected by board-to-board connect.

8. SVO-03 Switch

8.1. **SW1:** Push Switch

Currently, no features are assigned to the user.

8.2. **SW2:** DIP Switch

This is an 8-bit switch for setting various operation modes of SVO-03. Set the operation mode with No. 7 and No. 8.

8.2.1. USB input mode (#7: OFF, #8: ON)

Number	Name	Turns OFF	Turns ON
1	Reserved	OFF	--
2	Reserved	OFF	--
3	Reserved	OFF	--
4	Board Number bit0	Specify the board number recognized by SVOGenerator.	
5	Board Number bit1		
6	Board Number bit2		
7	MODE 0	OFF	--
8	MODE 1	--	**ON**

8.2.2. HDMI input and parallel output mode (# 8: OFF)

Number	Name	Turns OFF	Turns ON
1	Bit Width 1	8 Bit	16 Bit / 24 Bit
2	Reserved	OFF	--
3	Bit Width 2	Normal	Force 32 Bit
4	UYVY/YUY2	UYVY	YUY2
5	RGB/YUV	YUV 4:2:2	RGB24
6	Resolution	1920x1080	1280x720
7	MODE 0	60 FPS	30 FPS
8	MODE 1	OFF	--

- If the output timing is set by software (SVOCtl), the settings of DIP switches 6 and 7 are ignored.

8.2.3. HDMI input and USB output mode (#7: ON, #8: ON)

Number	Name	Turns OFF	Turns ON
1	Reserved	OFF	--
2	Reserved	OFF	--
3	Reserved	OFF	--
4	UYVY/YUY2	UYVY	YUY2
5	RGB/YUV	YUV 4:2:2	RGB24
6	Resolution	1920x1080	1280x720
7	MODE 0	--	ON
8	MODE 1	--	ON

・ Set the frame rate on the HDMI output side.

9. SVO-03 LED

9.1. Overview of LED1-10

SVO-03 has implemented a total of 10 LEDs with two red LEDs and eight green LEDs, and it is represented by silk on the board as LED1 to 10. As a breakdown, led1 and LED10 are red, and each "CAM power" and "Power" are named as silk notation. The green Led2 is also named "Vsync" and has a silk notation. LED10 "Power" lights up when power is turned on. Other LED1 to 9 are illuminated and controlled from the FPGA.

9.2. Operating Status Monitor LED details

These are LEDs that indicate the operating status of the board or FPGA.

LED	Description
1	"(USB input mode, HDMI input and parallel output mode) It is a red LED with a silk notation "CAM POWER". When lit, indicates that VDDH power and VDDL power are being supplied to the target, and at the same time signal input / output to the target is possible via the level shifter. When the LED is off, the VDDH and VDDL power supplies are disabled and no signal is output to the target. (HDMI input and USB output mode) Always off.
2	(USB input mode, HDMI input and parallel output mode) This is an LED with silk notation "VSYNC". Turns on / off the V-Sync sync signal output to the target with a frequency divided by 3. When the output image is 30fps, it blinks 5 times per second. (HDMI input and USB output mode) Always off.
3	(USB input mode, HDMI input and parallel output mode) Indicates the reset state to the target. It goes off when image output to the target is possible. Lights when output to the target is being prepared, or when image output to the target is not possible due to some problem. (HDMI input and USB output mode) Always off.

4	(USB input mode, HDMI input and parallel output mode) Lights when the pixel clock is output to the target. (HDMI input and USB output mode) Always off.
5	(USB input mode, HDMI input and parallel output mode) Lights when the pixel clock output to the target is locked. When the pixel clock is generated from the FPGA built-in clock generator, it lights up when the entire frequency synthesis DCM, PLL, etc. are locked. (HDMI input and USB output mode) Always off.
6	(USB input mode, HDMI input and parallel output mode) Lights when external clock input is selected. (HDMI input and USB output mode) Always off.
7	(USB input mode, HDMI input and parallel output mode) When the internal integrated video sync signal source is being driven, the V-Sync sync signal is turned ON / OFF at a frequency divided by 3. The blinking state of this LED does not necessarily indicate image output to the target. (HDMI input and USB output mode) When the FPGA is outputting UVC frames to FX3, the FV sync signal is turned ON / OFF with a period of 3 divided.
8	Lights when an image stored in the frame memory is loaded for output to the target. The lighting state of this LED does not necessarily indicate image output to the target.
9	(USB input mode) Flashes when the image source is input to the FPGA. Blinks when a large amount of data packets such as images are input from the USB port. (HDMI input and parallel output mode, HDMI input and USB output mode) Flashes when the source image is input from HDMI to the FPGA. Turns the V-Sync sync signal from the HDMI receiver ON / OFF at a frequency divided by 3.

10. Check terminal

10.1. **TP2**: “VDDH” check pin (red)

Check pin used when adjusting VDDH.

10.2. **TP4**: “VDDL” check pin (red)

Check pin used when adjusting VDDL.

10.3. **TP1 / 3 / 5 / 6**: Voltage check terminal (red)

Check terminal for each power supply voltage required for SVO-03 board operation. In normal use, there is no need to check. Also, do not remove power from this check terminal to supply power to the external module.

10.4. **TP7 / 8 / 9 / 10**: “GND” check terminal (black)

Use as GND pin for VDDH and VDDL adjustment.

10.5. **TP11 to 33**: IO signal check terminal (yellow)

Target signal check terminal. Silk of each signal is stamped. Use this when connecting measuring instruments.

11. Target Power Supply VDDH、VDDL

11.1. VDDH

Use VDDH with the camera module or the internal power supply of the target.

Adjust with RV1 mounted on the SVO-03 board. It can be adjusted in the range of 1.6V to 4.2V.

The default setting is + 3.3V.

11.2. VDDL

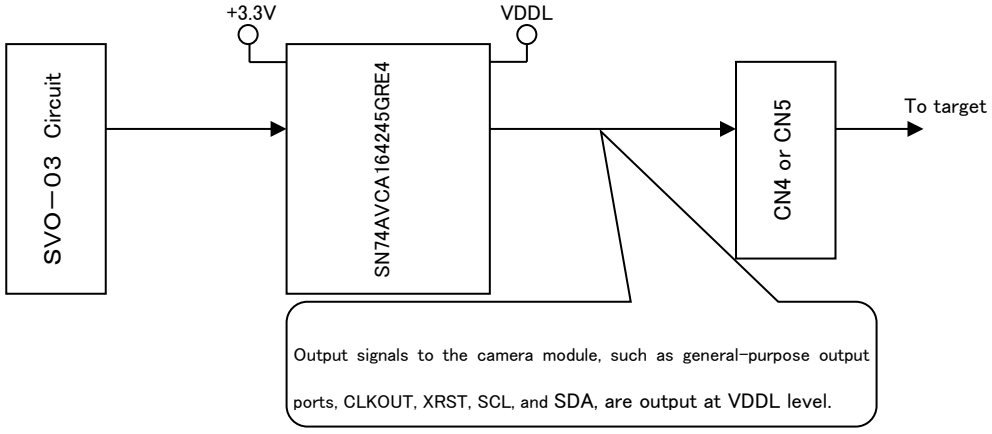
VDDL is a power supply for the IO signal level of targets such as camera modules.

Adjust with RV2 mounted on SVO-03 board. It can be adjusted in the range of 1.6V to 4.2V.

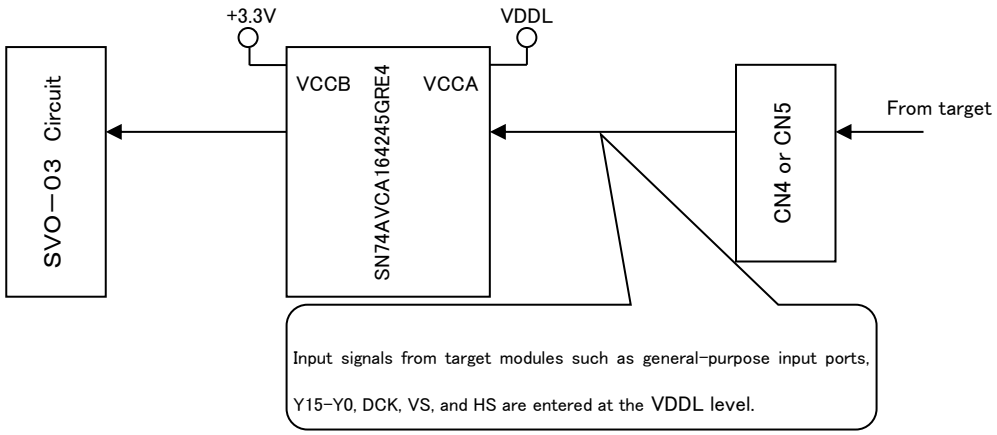
However, the recommended operating condition of the level shifter that converts the IO voltage to the target is in the range of 1.40V to 3.60V.

The default setting is + 3.30V. The schematic input / output circuit from the target is as follows.

11.3. Schematic diagram of output circuit



11.4. Schematic diagram of input circuit



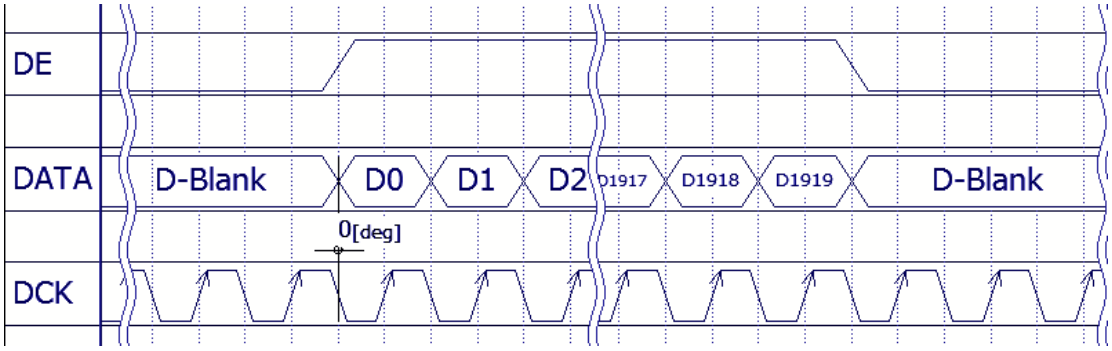
- **For the electrical specifications of the level shift IC (SN74AVCA164245GRE4), please download the datasheet from the Texas Instruments company HP and see. If you have any questions, please contact our sales officer.**

12. DCK output SDR/DDR mode settings

The DCK (pixel clock) output can be switched to DDR (Double data rate) In addition to the normal SDR (Single data rate) output. For high data transfer rate image output such as 1080p/60fps, when transferring with a standard data width of 16bit, the SDR clock output requires more than 100MHz DCK output, such as 148.5 [MHz]. This was difficult due to the limitations of the output circuit on the board. The DDR setting of the DCK output allows the data bus bit rate to be 148.5 [Mbps], lowering the DCK clock frequency to 1/2 74.25 [MHz]. This allows the image transfer of 1080p/60fps with a pin arrangement of the standard 16bit data width without exceeding the board constraints.

The DCK clock output setting allows you to set four modes in DDR in addition to the two modes in traditional SDR. The details of each mode are shown below.

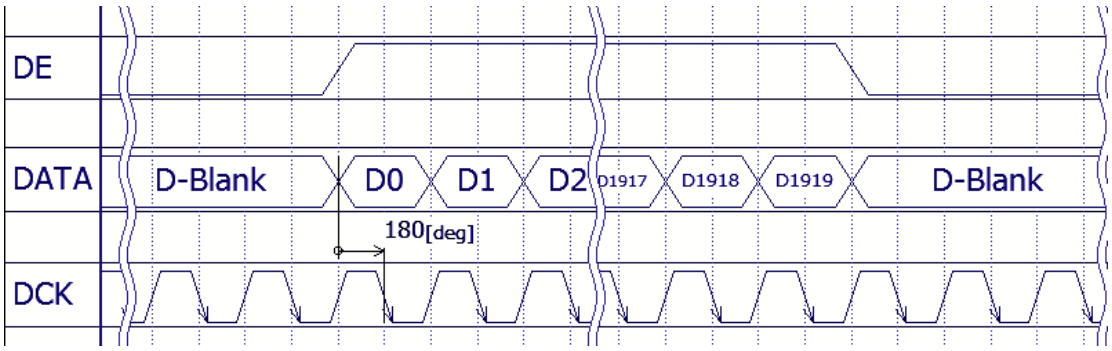
12.1. SDR-Mode0(pos-edge)



The most common DCK output setting. Drive data bus and synchronization signals at the Negative (Trailing)-Edge (falling edge) so that the target can be sampled at positive (Leading)-Edge (rising edge) in SDR.

The rising arrow in the DCK of the timing chart diagram indicates that the edge is for sampling when viewed from the target. In addition, as a synchronous signal, only the DE signal is shown, but other synchronous signals such as HS/VS/FI are similar to the DE signal.

12.2. SDR-Mode1(neg-edge)

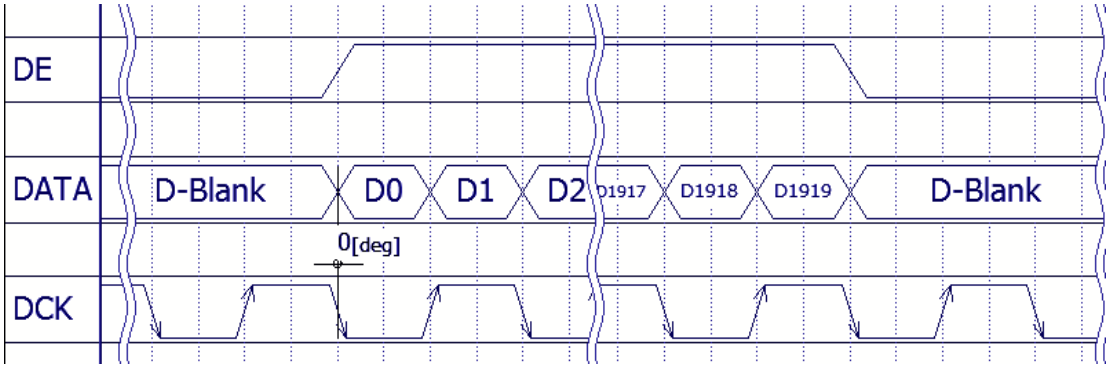


The DCK output to the SDR-Mode0 is a reversed clock or a 180 ° phase shifted relationship. Drive data bus and synchronization signals at the Positive (Leading)-Edge (rising edge) so that the target can be sampled at the negative (Trailing)-Edge (falling edge) in SDR.

The down arrow in the DCK of the timing chart diagram is the edge for sampling when viewed from the target. In addition, as a synchronous signal, only the DE signal is shown, but other synchronous signals such as HS/VS/FI are similar to the

DE signal.

12.3. DDR-Mode0(0°)

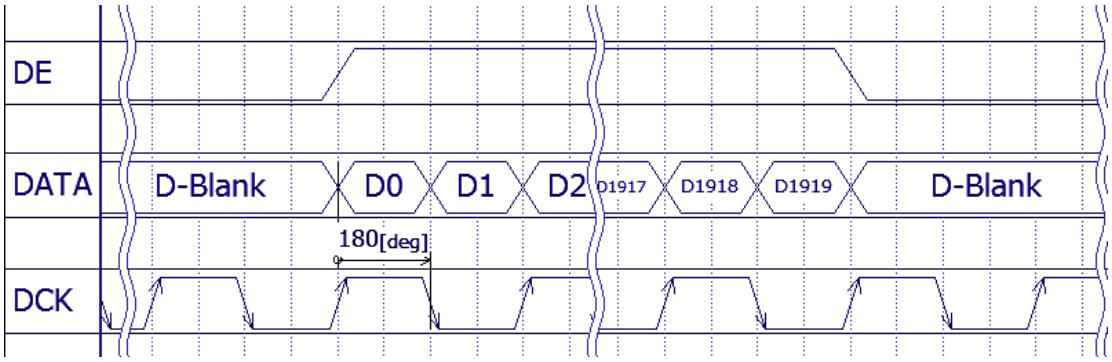


In DDR output settings, drive the DCK output so that the target samples the leading data with the rising edge and subsequent data on the falling edge. The DCK output and the data and synchronization signal edges are phase-aligned.

In DDR output, the data and the synchronous signal output are driven by an internal clock of twice the frequency for DCK. It becomes a phase pair of the preceding data (even number in the data bus of the figure) and the subsequent data (odd number). The clock and data edge phases are aligned in this mode. Since the preceding data is sampled at the rising edge as well as the SDR-Mode0, and it appears to be driving at the falling edge, it is a phase 0 ° as the basis for DDR-Mode.

The rise/fall arrows in the DCK of the timing chart diagram indicate that the edge is for sampling when viewed from the target. In addition, as a synchronous signal, only the DE signal is shown, but other synchronous signals such as HS/VS/FI are similar to the DE signal.

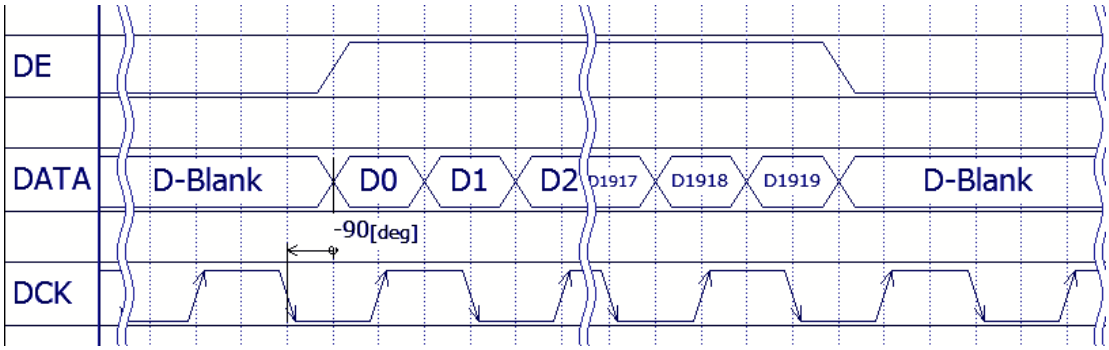
12.4. DDR-Mode1(180°)



In DDR output settings, the DCK output is a reversed clock for DDR-Mode0, or a 180 ° phase shift relationship. Drive the DCK output so that the target samples the preceding data at the falling edge and samples the trailing data on the rising edge. The DCK output and the data and synchronization signal edges are phase-aligned.

The rise/fall arrows in the DCK of the timing chart diagram indicate that the edge is for sampling when viewed from the target. In addition, as a synchronous signal, only the DE signal is shown, but other synchronous signals such as HS/VS/FI are similar to the DE signal.

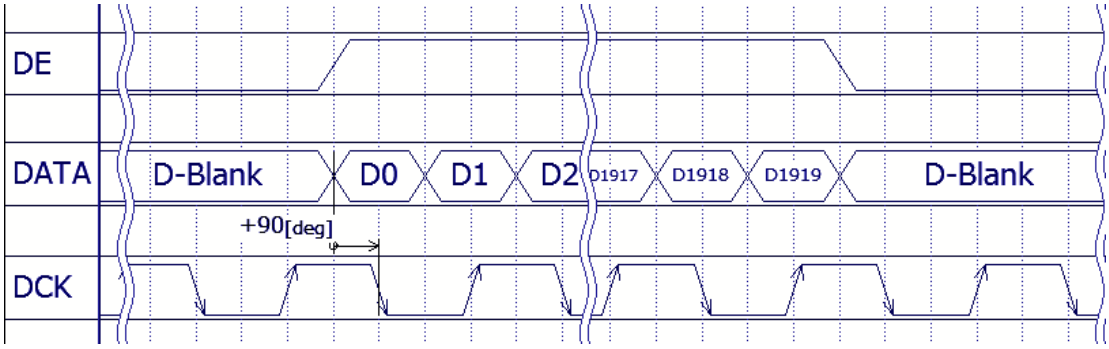
12.5. DDR-Mode2(-90°)



In DDR output settings, DCK is a-90 ° phase-shifted relationship to the DDR-Mode0 output. Drive the DCK output so that the target samples the preceding data at the rising edge and samples the trailing data at the falling edge. Sampling at the center of the eye pattern from the target view. For this reason, the DCK output is the-90 ° shifted output to the edge of the data and the synchronization signal.

The rise/fall arrows in the DCK of the timing chart diagram indicate that the edge is for sampling when viewed from the target. In addition, as a synchronous signal, only the DE signal is shown, but other synchronous signals such as HS/VS/FI are similar to the DE signal.

12.6. DDR-Mode3(+90°)



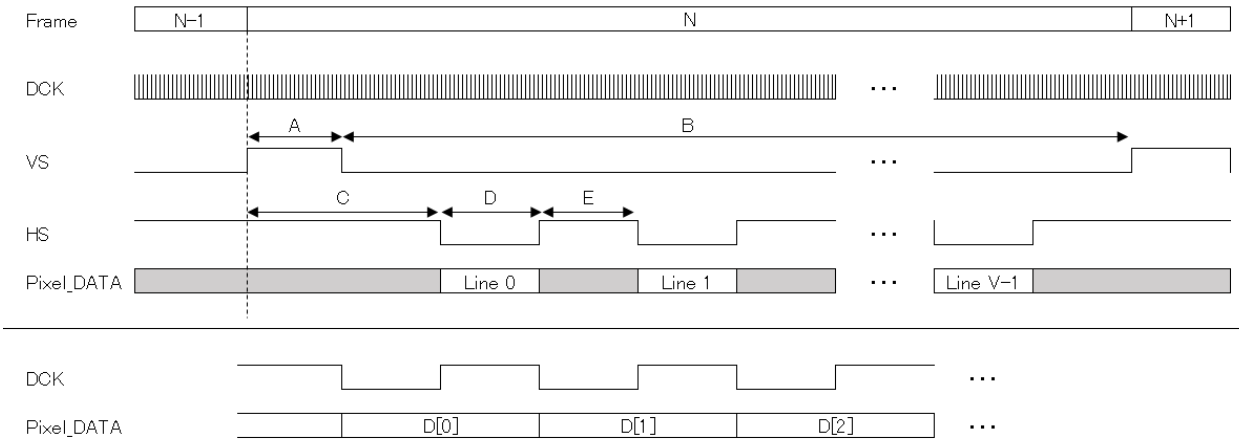
In DDR output settings, the DCK output is a + 90 ° phase-shifted relationship to the DDR-Mode0. Drive the DCK output so that the target will sample the preceding data at the falling edge and sample subsequent data at the rising edge. Sampling at the center of the eye pattern from the target view. For this reason, the DCK output is the-90 ° shifted output to the edge of the data and the synchronization signal.

The rise/fall arrows in the DCK of the timing chart diagram indicate that the edge is for sampling when viewed from the target. In addition, as a synchronous signal, only the DE signal is shown, but other synchronous signals such as HS/VS/FI are similar to the DE signal.

13. Output format details for HDMI input and parallel output mode

In HDMI input and parallel output modes, timing such as pixel clock and blanking period is fixed according to the frame format. If fine timing adjustment is required, it is necessary to use the timing setting file from SVOCtl.

13.1. List of signal lines and timing



- Polarity
- VS, HS: Negative logic (low active), change at the falling edge of DCK
- Pixel_DATA: Change at the fall of DCK.

Resolution	1280x720			1920x1080		1280x720		1920x1080
FPS	30		60	30	60	30	60	30
Format	YUV4:2:2					RGB24		
Bit Width	8	16			32	24		
fDCK [MHz]	74.25	37.125	74.25	74.25	74.25	37.125	74.25	74.25
A [DCKs]	99000	8250		11000	44160	8250		11000
B [DCKs]	2376000	1229250		2464000	1192320	1129250		2464000
C [DCKs]	99740	41510		90392	44304	41510		90392
D [DCKs]	2560	1280		1920	960	1280		1920
E [DCKs]	740	370		280	144	370		280

13.2. Output data configuration table

Format	YUV4:2:2						RGB24
Bit Width	8	8	16	16	32	32	24
DIP SW 4 (UYVY/YUY2)	OFF	ON	OFF	ON	OFF	ON	OFF
Pixel_DATA [31:24]	–	–	–	–	V	Y	–
Pixel_DATA [23:16]	–	–	–	–	Y	V	R
Pixel_DATA [15:8]	–	–	U->V	Y	U	Y	B
Pixel_DATA [7:0]	U->Y->V->Y	Y->U->Y->V	Y	V->U	Y	U	G

14. Notes

For proper use of this board, be sure to follow the following precautions.

1. If you want to connect or remove the target, be sure to turn on the SVO-03 board to the "OFF" state.
2. For the power supply to the board, read the 2.1 and 2.2 chapters carefully and connect to a PC that can fully secure the current capacity.
3. The contents of this document may be changed in the future without notice.
4. Reprinting of part or the whole of the contents of this document is strictly forbidden.
5. Through extreme care has been taken in preparing this document, if you find any ambiguous points or errors, or if you would like to make any comments on the document itself or its content, please contact to sv-support@net-vision.co.jp.

15. Appendix

15.1. CN2: USB3.0 Connector

USB 3.0 connector to connect to the host PC. A commercially available USB 3.0 cable is available. This connector is used for power supply of SVO-03.

connector		USB30B-09K-PC: JC Electronics Corporation					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	VBUS	IN	+ 5v Bus Power	2	D-	I/O	USB 2.0 Differential Pair-
3	D+	I/O	USB 2.0 Differential Pair+	4	GND	-	GND (Power)
5	SSRX-	IN	USB 3.0 receiver Differential pair -	6	SSRX+	IN	USB 3.0 receiver Differential pair +
7	GND DRAIN	-	GND (Signal)	8	SSTX-	OUT	USB 3.0 Transmission Differential pair -
9	SSTX+	OUT	USB 3.0 Transmission Differential pair +				

15.2. CN3: HDMI Connector

This connector is used to connect the HDMI monitor and the like through an HDMI cable.

connector		5-1903015-1: TE Connectivity					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	D2+	IN	TMDS Data 2+	2	D2 shield	-	TMDS Data 2 shield
3	D2-	IN	TMDS Data 2-	4	D1+	IN	TMDS Data 1+
5	D1 shield	-	TMDS Data 1 shield	6	D1-	IN	TMDS Data 1-
7	D0+	IN	TMDS Data 0+	8	D0 shield	-	TMDS Data 0 shield
9	D0-	IN	TMDS Data 0-	10	CLK+	IN	TMDS CLK +
11	CLK shield	-	TMDS CLK shield	12	CLK-	IN	TMDS CLK -
13	CEC	I/O	CEC Data	14	Utility	-	Utility

15	DDCSCL	I/(O)	DDC CLK	16	DDCSDA	I/O	DDC Data
17	GND	-	-	18	+5V	IN	+5V Power
19	HPD	OUT	Hot Plug Detection				

15.3. **CN6:** FPGA-JTAG Connector

The JTAG port used to write to the SPI-ROM of the FPGA bit stream or to debug a running FPGA. You do not need to use it in normal operation.

※The direction is seen from the FPGA.

Connector		A3B-14PA-2DSA(71): HRS					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	GND	-		2	VREF	OUT	Reference Voltage (3.3V)
3	GND	-		4	TMS	IN	JTAG-TMS
5	GND	-		6	TCK	IN	JTAG-TCK
7	GND	-		8	TDO	OUT	JTAG-TDO
9	GND	-		10	TDI	IN	JTAG-TDI
11	GND	-		12	NC	-	Disconnected
13	GND	-		14	NC	-	Disconnected

- **We do not guarantee the operation when you use it.**

15.4. Signal name and video signal assignment table

Pin#	Name	8bit	16bit	24bit	32bit
3	P0	General output port 0	General output port 0	Pixel_DATA16 (R0)	Pixel_DATA16
5	P1	General output port 1	General output port 1	Pixel_DATA17 (R1)	Pixel_DATA17
7	P2	General output port 2	General output port 2	Pixel_DATA18 (R2)	Pixel_DATA18
9	P3	General input port 0	General input port 0	General input port 0	Pixel_DATA24
11	P4	General input port 1	General input port 1	General input port 1	Pixel_DATA25
23	Y0	Pixel_DATA0	Pixel_DATA0	Pixel_DATA0 (B0)	Pixel_DATA0
25	Y1	Pixel_DATA1	Pixel_DATA1	Pixel_DATA1 (B1)	Pixel_DATA1
27	Y2	Pixel_DATA2	Pixel_DATA2	Pixel_DATA2 (B2)	Pixel_DATA2
29	Y3	Pixel_DATA3	Pixel_DATA3	Pixel_DATA3 (B3)	Pixel_DATA3
31	Y4	Pixel_DATA4	Pixel_DATA4	Pixel_DATA4 (B4)	Pixel_DATA4
33	Y5	Pixel_DATA5	Pixel_DATA5	Pixel_DATA5 (B5)	Pixel_DATA5
35	Y6	Pixel_DATA6	Pixel_DATA6	Pixel_DATA6 (B6)	Pixel_DATA6
37	Y7	Pixel_DATA7	Pixel_DATA7	Pixel_DATA7 (B7)	Pixel_DATA7
41	Y8	--	Pixel_DATA8	Pixel_DATA8 (G0)	Pixel_DATA8
42	Y9	--	Pixel_DATA9	Pixel_DATA9 (G1)	Pixel_DATA9
43	Y10	--	Pixel_DATA10	Pixel_DATA10 (G2)	Pixel_DATA10
44	Y11	--	Pixel_DATA11	Pixel_DATA11 (G3)	Pixel_DATA11
45	Y12	--	Pixel_DATA12	Pixel_DATA12 (G4)	Pixel_DATA12
46	Y13	--	Pixel_DATA13	Pixel_DATA13 (G5)	Pixel_DATA13
47	Y14	--	Pixel_DATA14	Pixel_DATA14 (G6)	Pixel_DATA14
48	Y15	--	Pixel_DATA15	Pixel_DATA15 (G7)	Pixel_DATA15
50	P5	General input port 2	General input port 2	General input port 2	Pixel_DATA26
51	P6	General input port 3	General input port 3	General input port 3	Pixel_DATA27
52	P7	General input port 4	General input port 4	General input port 4	Pixel_DATA28
53	P8	General input port 5	General input port 5	General input port 5	Pixel_DATA29
54	P9	General input port 6	General input port 6	General input port 6	Pixel_DATA30
55	P10	General input port 7	General input port 7	General input port 7	Pixel_DATA31
56	P11	General output port 3	General output port 3	Pixel_DATA19 (R3)	Pixel_DATA19
57	P12	General output port 4	General output port 4	Pixel_DATA20 (R4)	Pixel_DATA20
58	P13	General output port 5	General output port 5	Pixel_DATA21 (R5)	Pixel_DATA21
59	P14	General output port 6	General output port 6	Pixel_DATA22 (R6)	Pixel_DATA22
60	P15	General output port 7	General output port 7	Pixel_DATA23 (R7)	Pixel_DATA23